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Design of Storage Element for Low Power VLSI System

M. Guru Santhana Bharathi[1], P. Nagarajan[2]

[1] P.G.Scholar, Department of Electronics and Communication Engineering, PSNA College of Engineering and Technology, Dindigul, Tamilnadu, India. z

[2] Asst. Prof, Department of Electronics and Communication Engineering, PSNA College of Engineering and Technology, Dindigul, Tamilnadu, India. Email Id:nagarajan.pandiyan@gmail.com

Abstract- The storage elements are major power consuming component in VLSI system. The power reduction of storage element leads to reduction of global power consumption of VLSI system. In this paper, a Proposed single edge triggered (SET) and a Proposed double edge triggered (DET) logic module flip-flops are modeled and implemented by using TannerEDA. The DET offers a power reduction up to 13.34% compared to the conventional flip-flops. A new Proposed SET offers the power consumption up to 14.28% compared to conventional flip-flops and 9.34% power improvement compare with Proposed DET. The performance comparison has been made in a GENERIC LIBRARAY 0.25 µm ,0.18 nm TSMC VLSI process and 0.18 µm CMOS VLSI process , shows the Proposed SET & DET is power efficient flip-flop model and well suited for modern low power VLSI system design.

Index Terms-Logic, Flip-flops, High speed, Low-power.

1. Introduction

Technology and speed are always moving forward, from low scale integration to large scale integration. So, the system requires large number of components. In order to reduce the no of components we are using flip-flops. Semi dynamic flip-flop (SDFF) and Hybrid latch flip-flop (HLFF) are considered as the classic high performance flip-flops. These flip-flops that combines the merits of static and dynamic structures in hybrid architecture. In SDFF, only one transistor driven by the data input greatly helps to reduce pipeline overhead.

A flip-flop architecture named cross charge control flip-flop (XCFF), which has considerable advantages over SDFF and HLFF in both power and speed. But XCFF has some drawbacks, due to redundant power dissipation that results when the data does not switch for more than one clock cycles. XCFF is not very efficient due to susceptibility to charge sharing at the internal dynamic nodes.

In this paper, we propose a new Proposed SET and DET Flip-flops.Both of them eliminate the drawbacks of XCFF. SET presents a speed, area, and power efficient method to reduce the pipeline overhead. The performance of modern high performance flip-flops are compared with that of conventional flip-flops at different data activity. The post layout simulation results in GENERIC LIBRARY 0.25 µm, 0.18 nm TSMC process and 0.18µm CMOS process show that the SET saves 8% and 10% of the total power dissipated at 50% and 25% data activities, respectively when compared with XCFF. The proposed DET has a maximum power reduction of about 27% compared to its counterparts in SDFF.

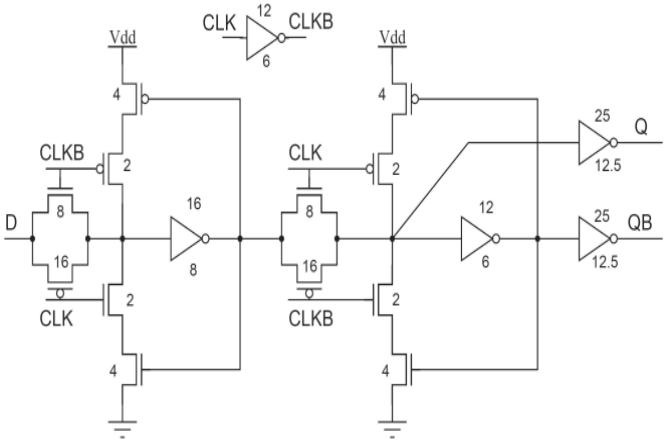

Fig 1. PowerPC 603 flip-flop.

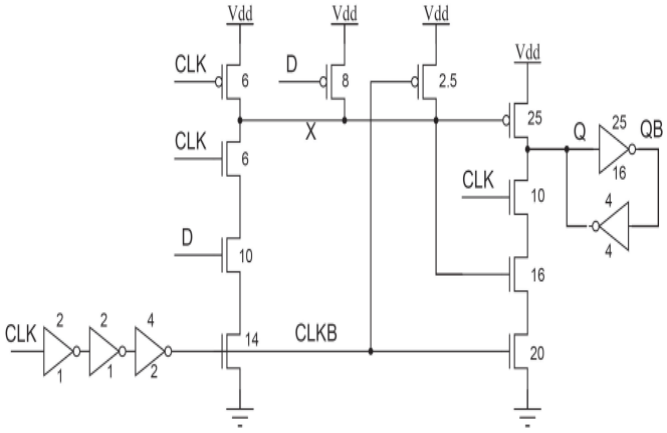

Fig .2 HLFF

The master-slave designs, such as the transmission gate based master-slave flip-flop such as the PowerPC 603 master-slave latch dissipate comparatively lower power and have a low clock-to-output (CLK-Q) delay.

In a synchronous system, the delay overhead associated with the latching elements is expressed by the data-to-output (D-Q) delay rather than CLK-Q delay. Here, D-Q delay refers to the sum of CLK-Q delay and the setup-time of the flip-flop.

ISSN 2348 - 7968

But the static designs lack a low D-Q delay because of their large positive setup time. Also, most of them are susceptible to flow-through resulting from CLK overlap.

PowerPC 603 is one of the most efficient classic static structures. It has the advantages of having a low-power keeper structure and a low latency direct path. As mentioned earlier, the large D-Q delay resulting from the positive setup time is one of the disadvantages of this design. Also, the large data and CLK node capacitances make the design inferior in performance.

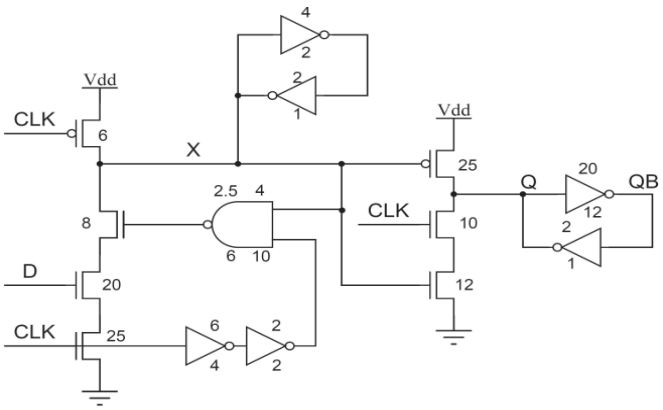

Fig 3. Semi dynamic flip-flop.

The second category of the flip-flop design, the dynamic flip-flops includes the modern high performance flip-flops There are purely dynamic designs as well as pseudo-dynamic structures. The latter, which has an internal precharge structure and a static output, deserves special attention because of their distinctive performance improvements. They are called the semi-dynamic or hybrid structures, because they consist of a dynamic frontend and a static output. HLFF and SDFF fall under this category. They benefit from the CLK overlap to perform the latching operation. SDFF is the fastest classic hybrid structure, but is not efficient as far as power consumption is concerned because of the large CLK load as well as the large precharge capacitance. HLFF is not the fastest but has a lower power consumption compared to the SDFF. The longer stack of nMOS transistors at the output node makes it slower than SDFF and causes large hold-time requirement. This large positive hold time requirement makes the integration of HLFF to complex circuits a difficult process. Also it is inefficient in embedding logic.

The major sources of power dissipation in the conventional semi-dynamic designs are the redundant data transitions and large precharge capacitance. Many attempts have been made to reduce the redundant data transitions in the flip-flops. The conditional data mapping flip-flop (CDMFF) is one of the most efficient among them. It uses an output feedback structure to conditionally feed the data to the flip-flop. This reduces overall power dissipation by eliminating unwanted transitions when a redundant event is predicted. Since there are no added transistors in the pull-down nMOS stack, the speed performance is not greatly affected. But the presence of three stacked nMOS transistors at the output node, similar to HLFF, and the presence of conditional structures in the critical path increase the hold time requirement and D-Q delay of the flip-flop. Also, the additional transistors added for the conditional circuitry make the flip-flop bulky and cause an increase in power dissipation at higher data activities.

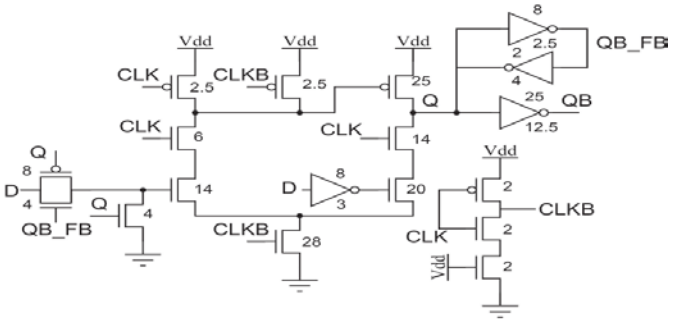

Fig 4. CDMFF.

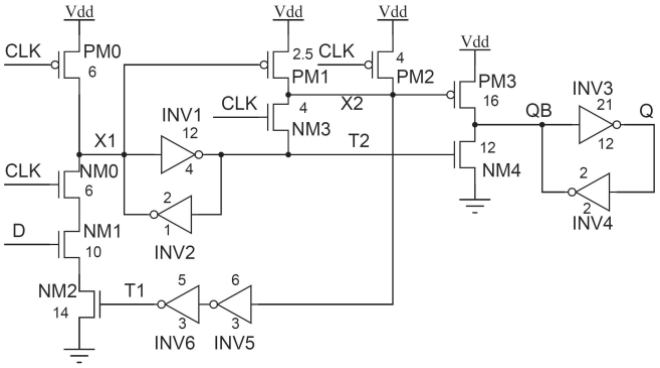

Fig 5. XCFF.

Fig. 6 shows the proposed DDFF architecture. Node *X*1 is pseudo-dynamic, with a weak inverter acting as a keeper, whereas, compared to the XCFF, in the new architecture node Proposed DDFF. *X*2 is purely dynamic. An unconditional shutoff mechanism is provided at the frontend instead of the conditional one in XCFF. The operation of the flip-flop can be divided into two phases: 1) the evaluation phase, when CLK is high, and 2) the precharge phase, when CLK is low. The actual latching occurs during the 1–1 overlap of CLK and CLKB during the evaluation phase.

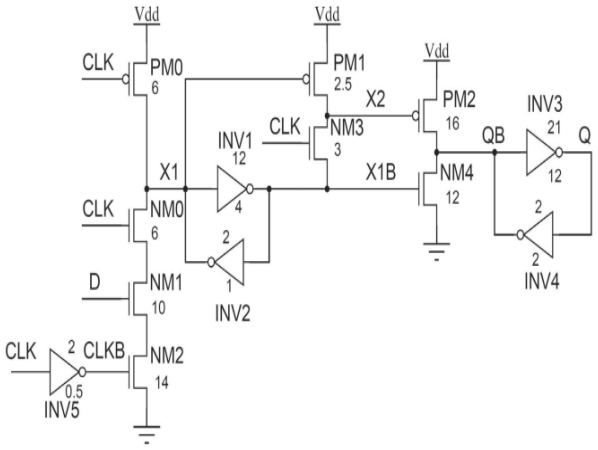

Fig 6. DDFF

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As mentioned earlier, the major advantage of the SDFF is the capability to incorporate complex logic functions efficiently. The efficiency in terms of speed and area comes from the fact that an *N*-input function can be realized in a positive edge triggered structure using a pull-down network (PDN) consisting of *N* transistors. Compared to the discrete combination of *N* a static gate and a flip-flop, this embedded structure offers a very fast and small implementation. Although SDFF is capable of offering efficiency in terms of speed and area, it is not a good solution as far as power consumption is concerned. Not too many attempts have been made to design a flip-flop, which can incorporate logic efficiently in terms of power, speed and area. Various functions have been embedded into the proposed design to analyze the performance of the structure in terms of power and speed. Since SDFF is considered to be the benchmark of comparison, it was also simulated under similar conditions when embedded with the same functions. SDFF has a fast non inverting output and a slow inverting output, whereas the proposed design has a fast inverting output and a slow non inverting output. In order to have a fair comparison of delay, inverting and non inverting outputs, respectively were considered for SDFF and the proposed design. SCCER in all the above designs was designed using three inverters for generating sampling window so as to obtain the worst case timing results of the design.

2. Proposed Single Edge Triggered Flip-Flop (SET)

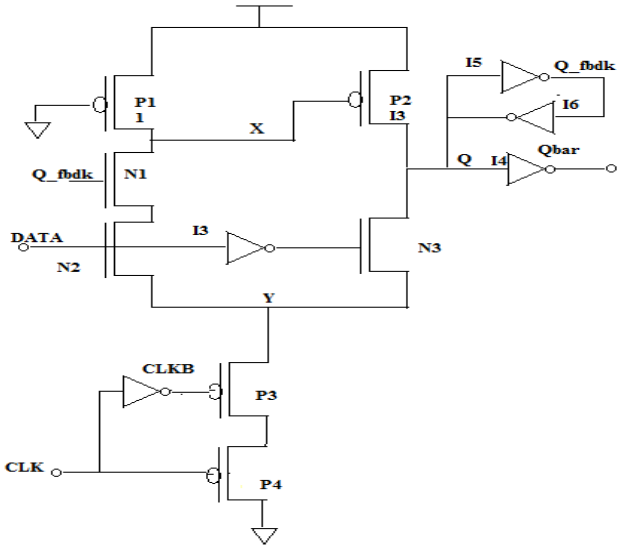

Fig 7: Single Edge Triggered Flip-flop.

Fig 7 shows a single edge triggered (SET) flip-flop. In SET the transistor N1, controlled by the output QB, provides conditional capturing. The right-hand side evaluation path is static and does not require conditional capturing. Placing N1 above N2 in the stack reduces the charge sharing. In this design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains pMOS transistors P3 and P4 connected in series. In order to eliminate superfluous switching at node an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through four transistors in series, i.e., P4 through N2, while combating with the pull up transistor P1. A powerful pull-down circuitry isthus needed to ensure node X can be properly discharged. This implies wider P4 and P3 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

By Using Generic Library 0.25, TSMC 0.18 and CMOS 0.18 technologies with a supply voltage of 0.5v the Proposed SET flip-flop are designed and reduce the largest amount of power compared to all other conventional flip-flops.

3. Proposed Double Edge Triggered Flip-flop (DET)

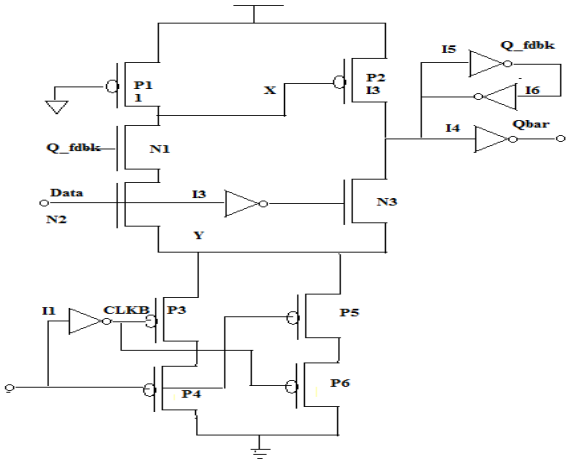

Fig 8: Double Edge Triggered Flip-flop.

Fig 8 shows a Double edge triggered(DET) Flip-flop.the transistor N1, controlled by the output QB, provides conditional capturing. The right-hand side evaluation path is static and does not require conditional capturing. Placing N1 above N2 in the stack reduces the charge sharing. In this design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains pMOS transistors P3 & P4 and P5 & P6 connected in series. P3 & P4 are connected parallel to P5 & P6. In order to eliminate superfluous switching at node an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node X is discharged through six transistors in series, i.e., P6 through N2, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider P4 & P3 and P6 & P5 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

By Using Generic Library 0.25, TSMC 0.18 and CMOS 0.18 technologies with a supply voltage of 0.5v the Proposed DET flip-flop are designed and reduce the largest amount of

ISSN 2348 - 7968

FLIPFLOPS	POWER RESULTS (MICRO WATTS) WITH DIFFERENT TECHNOLOGIES								
	GENERIC LIBRARY 025			TSMC 018			CMOS 018		
	MIN	AVG	MAX	MIN	AVG	MAX	MIN	AVG	MAX
SDFF	4.29	5.39	6.06	5.19	5.93	6.48	5.24	6.09	7.73
HLFF	4.72	5.98	6.04	5.20	5.29	5.36	4.56	5.07	6.05
XCFF	4.49	5.19	6.49	4.61	5.13	5.54	5.48	6.11	6.29
PPFF 603	4.84	5.97	7.26	4.24	4.61	5.05	5.57	6.67	6.97
CDMFF	5.82	7.17	9.24	5.11	7.46	9.11	5.39	6.39	8.93
DDFF	5.64	7.06	9.42	5.62	6.56	8.85	5.85	6.88	7.81
PROPOSED SET*	2.06	3.17	3.77	2.89	3.01	3.62	2.65	2.89	3.58
PROPOSED DET*	2.81	3.55	3.79	2.89	3.04	3.69	2.65	3.11	3.65

power compared to all other conventional flip-flops and the results are tabulated in Table 1.

Table 1. Simulation Results of FFs.

*Proposed Flip-Flop Results

5. Conclusion

In this paper, a low power SET and DET flip-flop circuits were modeled and analyzed. The proposed SET eliminates the redundant power dissipation present in the XCFF. A comparison of the proposed flip-flops with the conventional flip-flops showed that it exhibits lower power dissipation along with comparable speed performances. The post-layout simulation results showed an improvement in power about 9.11% and 11.7% compared to the XCFF with DET and SET respectively. DET consumes less power compared to SET with considerable delay. The performance comparisons made in a Using Generic Library 0.25, TSMC 0.18 and CMOS 0.18 technologies process, shows the SCCER is power efficient flip-flop model and well suited for modern low power VLSI system design.

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