

A Theoretical description of Graphene based Transistors

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Abstract

Area, Power and Speed are the major concerns of the upcoming VLSI era. All of them must be reduced to a greater extent to yield a better device. Abiding Moore's law which states for every 18 months the number of transistors to be integrated on a single die gets double, area has become a prominent competent. Clock power contributes to 55% of the total power of the circuit which has to be ultimately reduced. Delay is the other elegant thing that has to be taken into account. Lesser the delay produced, better the performance of the circuit. Achieving success in all the three mentioned criteria has become a great deal in present day technologies.

Keywords: MOSFET, CNTFET, GNRFET, threshold voltage, area, power and delay.

1. Introduction

The observation made in 1965 by Gordon Moore, co-founder of Intel, the number of transistors per square inch on integrated circuits had doubled every year since the integrated circuit was invented as shown in Fig.1.1 Moore predicted that this trend would continue for the foreseeable future. In subsequent years, the pace slowed down a bit, but data density has doubled approximately every 18 months, and this is the current definition of Moore's law, which Moore himself has blessed. Most experts, including Moore himself, expect Moore's law to hold for at least another two decades.

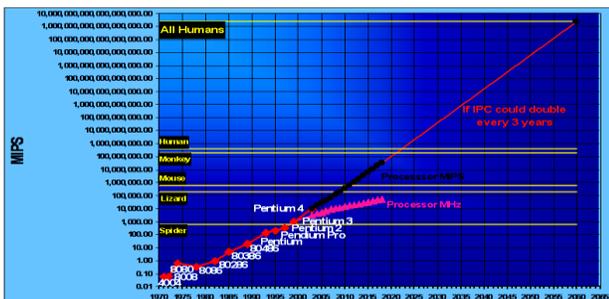


Fig. 1 Representation of Moore's law

2. Transistor Basics

A device composed of semiconductor material that amplifies a signal or opens or closes a circuit. Invented in 1947 at Bell Labs, transistors have become the key ingredient of all digital circuits, including computers. Today's microprocessors contains tens of millions of microscopic transistors. The first transistor was invented at Bell laboratories on December 6, 1947 by William Shockley (seated at Brattin's laboratory bench), John Bardeen (left) and Walter Brattin (right). This was perhaps the most important electronics event of 20th century, as it later made possible the integrated circuit and microprocessor that are the basis of modern electronics shown in Fig



Fig. 2 The first Transistor invented

2.1 Field Effect Transistor

The Field Effect Transistor is a device which enables us to use one electrical signal to control another. The voltage on (or current into/out of) one wire has the effect of controlling the ease with which current can move between the other two terminals. We can use this behavior to 'transfer' patterns of signal fluctuation from a small input signal to a larger output signal. All FETs have

a gate, drain, and source terminal. The size of the gate, length L in the diagram, is the distance between source and drain. The names of the terminals refer to their functions. The gate terminal may be thought of as controlling the opening and closing of a physical gate. This gate permits electrons to flow through or blocks their passage by creating or eliminating a channel between the source and drain. Electrons flow from the source terminal towards the drain terminal if influenced by an applied voltage. The body simply refers to the bulk of the semiconductor in which the gate, source and drain lie. Usually the body terminal is connected to the highest or lowest voltage within the circuit, depending on type.

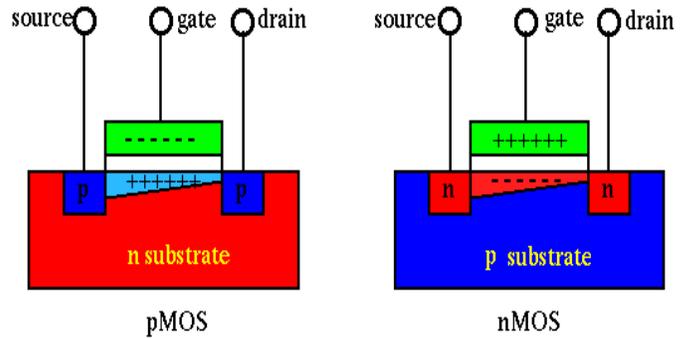


Fig. 4 pMOS and nMOS Transistors

3. MOSFET Technology

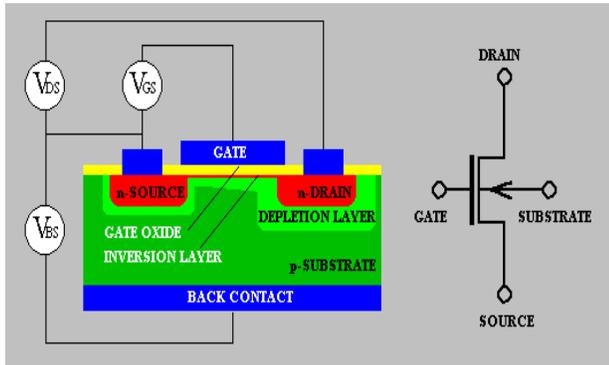


Fig. 3 Structure of a MOSFET

The basic principle of the MOSFET is that the source to drain current (sd current) is controlled by the gate voltage, or better, by the semiconductor at the semiconductor oxide interface. Thus the MOSFET is a voltage controlled current source as shown in Fig. 3. In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called an nMOSFET or a pMOSFET (also commonly nMos, pMos). The 'metal' in the name is now often a misnomer because the previously metal gate material is now often layer of polysilicon (polycrystalline silicon). Aluminum had been the gate material until the mid-1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates .

3.1 MOSFET Scaling

Over the past decades, the MOSFET is continually been scaled down in size; typical MOSFET channel lengths were once several micrometers , but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation as shown in Fig.5

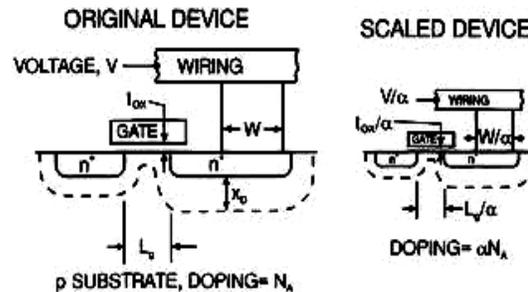


Fig. 5 Concept of MOSFET scaling

3.2 Drawbacks of MOSFET

Silicon based technology will reach its limits in 2020 when the channel length of MOSFET is below 10nm. For this reason, the semiconductor industry is looking for different materials and devices to integrate with the current silicon-based technology or maybe, in a long term future, even substitute it. Among the number of investigated solutions such as single-electron tunneling (set), rapid single-flux quantum logic, quantum cellular automata (QCA), carbon

Nanotube (CNT) and Graphene Nano ribbons (GNR), GNRs are a promising material. They have diameters of typically 1 to 3 nm but being long up to several microns. GNRs can be exploited to build both low-resistance high-strength interconnections and highly scalable low-power Graphene Nano Ribbon field-effect transistors (GNRFET) and single electron tunneling transistors one of the basic ideas is to replace the silicon MOSFETs with CNTFETs to overcome all the limitations of silicon MOSFETs.

4. Carbon Nanotube Field Effect Transistors (CNTFET's)

Carbon is the most versatile element in the periodic table, owing to the type, Strength and number of bonds it can form with many different elements. The properties of carbon are a direct consequence of the arrangement of electrons around the nucleus of the atom. Carbon in the solid phase can exist in three allotropic forms: graphite, diamond, and buckminsterfullerene. Graphite is made by layered planar sheets of sp^2 hybridized carbon atoms bonded together in a hexagonal network. Buckminsterfullerene, or fullerenes, are the third allotrope of carbon and consist of a family of spheroid or cylindrical molecules with all the carbon atoms sp^2 hybridized

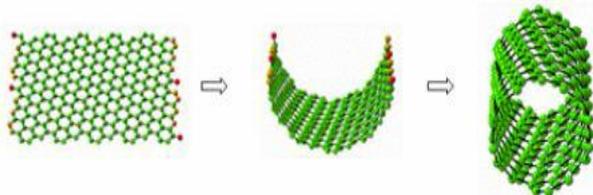


Fig. 6 Formation of CNT from Graphene sheet

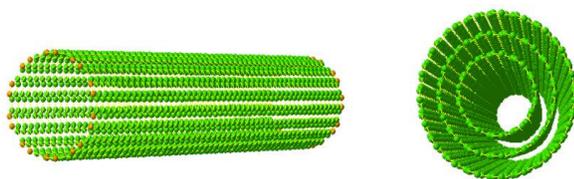


Fig. 7 Single Walled and Multi Walled CNT

4.1 CNTFET

The scaling down of devices has been the driving force in technological advances since late 20th century. However, as noted by ITRS 2009 edition, further scaling down has

faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and Variations in device structure and doping. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk MOSFET structure with a single carbon nanotube or an array of carbon nanotubes [29]. Carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure

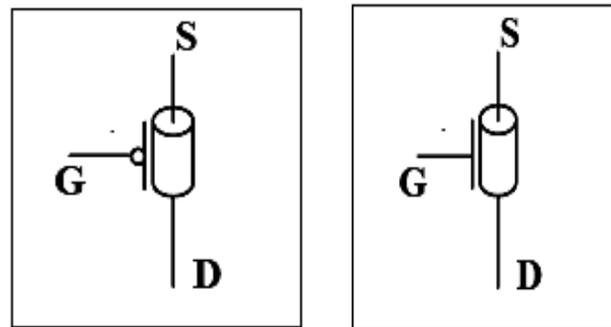


Fig. 8 p-type and n-type CNTFET

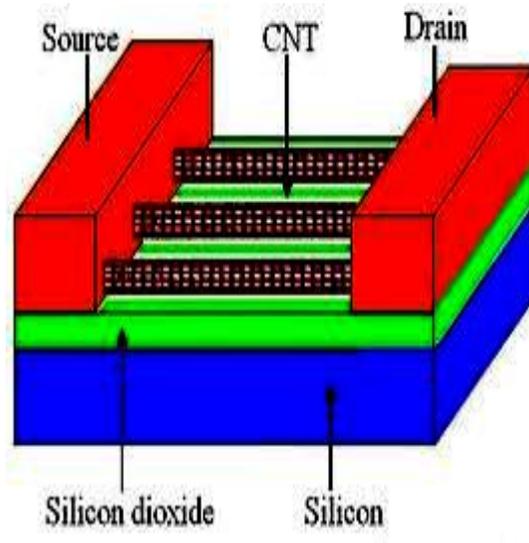


Fig. 9 Arrangement of CNT between Source and Drain

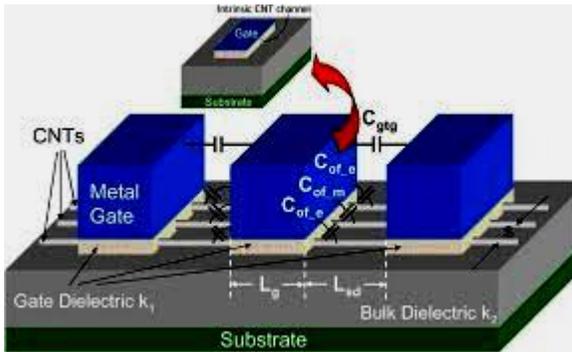


Fig. 10 A Typical CNTFET Device

4.2 Description of 32nm CNTFET Model

Table 1 : 32nm CNTFET Model Parameters

Device Parameter	Description	Value
Lch	Physical channel length.	32.0nm (Set by global parameter $L_{channel}$)
Lgeff	The mean free path in the intrinsic CNT channel region due to non-ideal elastic scattering.	200.0nm (Set by global parameter L_{ceff})
Lss	The length of doped CNT source-side extension region.	32.0nm (Set by global parameter L_{sd})
Ldd	The length of doped CNT drain-side extension region.	32.0nm (Set by global parameter L_{sd})
Efi	The Fermi level of the doped S/D tube.	0.6 eV (Set by global parameter E_{fo})
Kgate	The dielectric constant of high-k top gate dielectric material (planer gate).	16.0 (Set by global parameter K_{ox})
Tox	The thickness of high-k top gate dielectric material (planer gate).	4.0nm
Csub	The coupling capacitance between the channel region and the substrate (backgate effect).	20.0pF/m (for a 10 μ m thick SiO ₂)
Ccsd	The coupling capacitance	0.0pF/m (Set by

	between channel region and source/drain region.	global parameter C_{csd}
CoupleRatio	The percentage of C_{csd} that corresponds to the coupling capacitance between the channel and drain.	0.0 (Set by global parameter $CoupleRatio$)
Vfbn, Vfbp	Flatband voltage for n-CNFET and p-CNFET, respectively.	0.0eV, 0.0eV
Dout	The property of the drain-side output: 0: the drain output is connected to metal contact, 1: the drain output is connected to another CNFET directly.	0
Sout	The property of the source-side output: 0: the source output is connected to metal contact, 1: the source output is connected to another CNFET directly.	0
Pitch	The distance between the centers of two adjacent CNTs within the same device ¹ .	20.0nm
Wgate	The width of metal gate ² .	6.4nm (set by global parameter sub_pitch)
CNTPos	The position of CNT under the gate (only for Uniform Models): 0: the tube is in the middle and sees two adjacent neighbors, 1: the tube is at edge of the device and sees only 1 neighboring CNT.	1
(n1, n2)	The chirality of tube ³ .	(19, 0)
tubes	The number of tubes in the device.	1

Thus the above table clearly explains all the parameters used in the Carbon Nano Tube field Effect Transistors. The globally accepted value of each and every parameter of the CNTFET devices is also clearly described with proper notations. These values can be used up to the channel length of 10nm. The operating voltage and operating frequency used here is 0.9v and 1 Giga Hertz respectively.

5. Graphene Nano Ribbon Field Effect Transistors (GNRFET's)

5.1 Graphene Nano Ribbon Field Effect Transistor

Field-effect transistors using carbon-based Nano-materials have emerged as promising next-generation devices because of their out-standing electrical properties and integration capabilities via new fabrication techniques. The most studied are carbon nanotube FETs (CNFETs) and graphene Nano ribbon FETs (GNRFETs). Compared to cylindrical CNTs, GNRs can be grown through a silicon-compatible, transfer-free, and in situ process, thus having nonalignment and transfer-related issues as encountered by CNT-based circuits. A graphene Nano ribbon Field-Effect Transistor refers to a field-effect transistor that utilizes a single graphene sheet or an array of graphene sheets as the channel material instead of bulk silicon in the traditional MOSFET structure. It was first demonstrated in 2004, there have been major developments in GNRFETs which promise for an alternative material to replace silicon in future electronics.

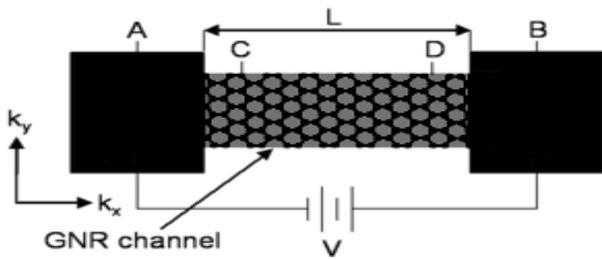


Fig. 11 operational description of GNRFET

5.2 Graphene

Graphene is crystalline allotrope of carbon. In graphene, carbon atoms are densely packed in a regular sp^2 -bonded atomic-scale chicken wire (hexagonal) pattern. Graphene can be described as a one-atom thick layer

of graphite. High-quality graphene is strong, light, nearly transparent and an excellent conductor of heat and electricity. Its interactions with other materials and with light and its inherently two-dimensional nature produce unique properties, such as the bipolar transistor effect, ballistic transport of charges and large quantum oscillations. The combination of familiarity, extraordinary properties and surprising ease of isolation enabled a rapid increase in graphene research. It has a very peculiar structure, being composed of a single layer of carbon atoms (only one atom thick) arranged in a grid which resembles common chicken wire. This structure grants graphene its exciting electronic properties: over this two-dimensional carbon Nano world, electrons move almost freely at very high speeds, acting like massless particles. For the electronic industry, this means more efficient devices that will be able to be built a lot smaller than what silicon allows.

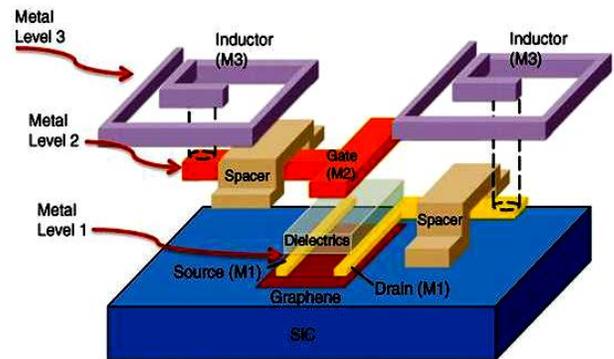


Fig. 12 Ballistic GNRFET (MOSFET like GNRFET)

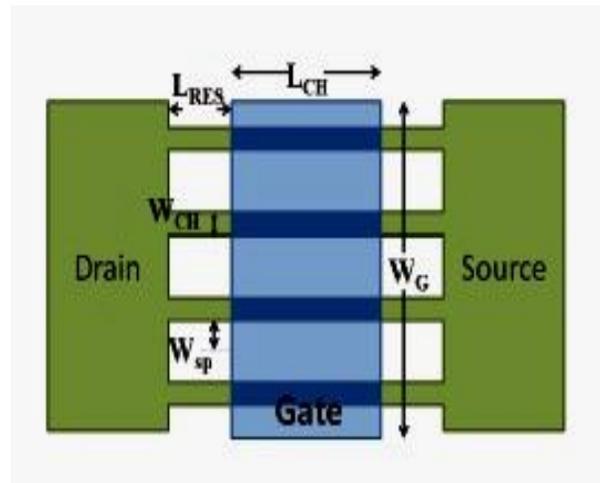


Fig. 13 Parameters Explanations of GNRFET

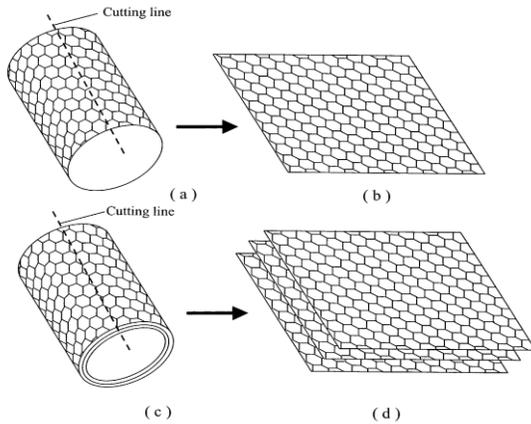


Fig. 14 Graphene Sheets

5.3 Advantages of GNRFET

It dissipates very less heat and can operate at terrifying speed of 400GHz. They have High current-carrying capacity and thermal conductivity. It is 100 times faster than MOSFET. Mobility of GNRFET is 200,000 cm²/vs whereas MOSFET and CNTFET are only 1400cm²/vs and 100,000cm²/vs. Range of temperature is 13°C whereas silicon is 55°C. Very expensive operations can be performed. Much lighter and sturdier than MOSFET. GNRFET can be used to create circuits that are almost superconducting, potentially speeding electronic components by as much as 1000 times. They have Excellent switching properties. GNRFET are stronger, stiffer, and less prone to failure than composites infused with carbon nanotubes or other nanoparticles. Strong bonding, very high density, Geometry and Easy interconnect steps are some of the advantages that is to be taken into account.

5.4 Description of 15nm GNRFET Model

Table 2 : 15nm GNRFET Model Parameters

Parameter	Specification
L	15nm
Tox	0.95nm
2*sp	2nm

nRIB	6
P	0
Dop	0.001
Gates_tied	0
Tox2	20nm
V _{DD}	0.4v

6. Conclusions

Thus the paper clearly illustrates the MOSFET technology in the beginning and describes the major disadvantages faced with the silicon based transistors. The later part of the paper gives the crystal clear ideologies about the carbon or graphene based transistors the CNTFET and the GNRFET. The advantages of graphene transistors over the silicon transistors are discussed. Hence from the above discussions it is been very clear that the future VLSI devices or components designed with CNTFET's and GNRFET's shows exemplary results in terms of Pwer, Delay and Area consumptions

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