Design of Low Power Adder and Multiplier Using Reversible Logic Gates

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Abstract

In this project reversible logic gates are designed. Reversible logic is a prominent technology in Quantum computing technology. The devices used by this technology operate at ultra high speed and consume very low power. In this work basic reversible logic gates are implemented using hardware description language. The Wallace tree multiplier is implemented using basic half adder and full adder using verilog. GCD processor is also implemented using verilog. The reversible logic gates are designed and a 4bit reversible adder, irreversible adder along multiplier is designed. Various foundry technologies are used for the design of layouts and comparison among these technologies is done. The least power dissipation technology is concluded. In this paper a 4x4 bit reversible multiplier circuit is proposed and designed. The proposed reversible multiplier is faster and has lower hardware complexity compared to the existing counterparts. It is also better than the existing counterparts in term of number of gates, garbage outputs and constant inputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "HNG". The reversible HNG gate can work singly as a reversible full adder. In this paper we use HNG gates to construct the reversible multiplier circuit. The proposed reversible multiplier circuit using HNG gate can multiply two 4-bits binary numbers. The proposed reversible 4x4 multiplier circuit can be generalized for NxN bit multiplication.

Keywords: Reversible gates, Power Dissipation, Verilog, Adder, Multiplier

1. Introduction

Reversible computing was started when the basis of thermodynamics of information processing was shown that conventional irreversible circuits unavoidably generate heat because of losses of information during the computation. The different physical phenomena can be exploited to construct reversible circuits avoiding the energy losses. One of the most attractive architecture requirements is to build energy lossless, small and fast quantum computers. Most of the gates used in digital design are not reversible for example NAND, OR and EXOR gates.

A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2x2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate which is not used as input to other gate or as a primary output is called garbage output.

In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication
processes have dramatically reduced the heat loss over the last decades. The power dissipation in a circuit can be reduced by the use of Reversible logic. Landauer’s [2] principle states that irreversible computations generates heat of K*Thln2 for every bit of information lost, where K is Boltzmann’s constant and T the absolute temperature at which the computation performed. Bennett [3] showed that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible.

A set of reversible gates are needed to design reversible circuit. Several such gates are proposed over the past decades. Arithmetic circuits such as Adders, Sub tractors, Multipliers and Dividers are the essential blocks of a Computing system. Dedicated Adder/Sub tractor circuits are required in a number of Digital Signal Processing applications. Several designs for binary Adders and Sub tractors are investigated based on Reversible logic. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic.

Pawel Kerntopf [20] explained multipurpose Reversible gates and example of efficient binary multipurpose reversible gates. Thapliyal and Ranganathan [5] proposed the design of Reversible Binary Sub tractor using TR Gate. The particular function like Binary Subtraction is implemented using TR gate effectively by reducing number of Reversible gates, Garbage outputs and Quantum Cost. Thapliyal and Ranganathan [6] presented a design of Reversible latches viz., D Latch, JK latch, T latch and SR latch that are optimized in terms of quantum cost, delay and garbage outputs. Lihui Ni et al., [7] described general approach to construct the Reversible full adder and can be extended to a variety of Reversible full-adders with only two Reversible gates. Irina Hashmi and Hafiz Hasan Babu [8] designed an efficient reversible barrel shifter which is capable of left shift/rotate used for high speed ALU applications.


Majid Mohammadi and Mohammad Eshghi [12] explained about the behavioral description and synthesis of quantum gates. To synthesize reversible logic circuits, V and V+ gates are shown in the truth table form and shown that bigger circuits with more number of gates can be synthesized. Rekha James et al.,[13] proposed an implementation of Binary Coded Decimal adder in Reversible logic, which is basis of ALU for reversible CPU.

VLSI implementations using one type of building block can decrease system design and manufacturing cost. Himanshu Thapliyal and Vinod [14] presented the Transistor realization of a new 4*4 Reversible TSG gate. The gate alone operates as a Reversible full adder. The Transistor realizations of 1-bit Reversible full adder, ripple carry adder and carry skip adder are also discussed. Himanshu Thapliyal and Srinivas [15] proposed a 3x3 Reversible TKS gate with two of its outputs working as 2:1 multiplexer.

The gate used to design a Reversible half adder and further used to design multiplexer based Reversible full adder. The multiplexer based full adder is further used to design Reversible 4x4 Array and modified Baugh Woolley multipliers.

Yvan Van Rentergem and Alexis De Vos [16] presented four designs for Reversible full-adder circuits and the implementation of these logic circuits into electronic circuitry based on C-MOS technology and pass-transistor design. The chip containing three different Reversible full adders are discussed. Mozammel Khan [17] proposed realizations of ternary half and full-adder circuits using generalized ternary gates. Mozammel Khan [18] discussed quantum realization of ternary Toffoli gate which requires fewer gates than the existing literature.

Abhinav Agrawal and Niraj Jha [19] presented 6 the first practical synthesis algorithm and tool for Reversible functions with a large number of inputs. It uses positive-polarity Reed-Muller decomposition at each stage to synthesize the function as a network. In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss lower the last decades. The power dissipation in a circuit can be reduced by the use of reversible logic.

According to Landauel’s principle states that irreversible computations generates heat of K*Thln2 for every bit of information lost, where K is Boltzmann’s constant and T the absolute temperature at which the computation performed. Bennett showed that if a computation is carried out in reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not results in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Several such gates are proposed over the past decades.
2. Reversible logic gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also in the synthesis of reversible circuits direct fan-out is not allowed as one-to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits.

Figure 1: Reversible Gate

A gate with k inputs and k outputs is called k*k gate. The gate/circuit that does not loose information is called reversible. The input vector and output vector of a reversible gate is as shown in equations (1) & (2).

Input Vector

$$I_k = (I_1, I_2, I_3, \ldots, I_{k-1}, I_k) \ldots \ldots (1)$$

Output Vector

$$O_k = (O_1, O_2, O_3, \ldots, O_{k-1}, O_k) \ldots \ldots (2)$$

3. Implementation of Reversible Gates

Reversible computation is related to other emerging technologies such as quantum computation, optical computing, and nanotechnologies that use a similar or slightly extended set of gates.

First implementations and fabrications of reversible logic in CMOS technology have also been accomplished. These exploit that reversible logic is particularly suitable when it comes to reuse of signal energy (in contrast to static CMOS logic that sinks the signal energy with each gate), and, when using adiabatic switching to switch transistors in a more energy efficient way.

In fact, reversible circuits have shown that such implementations have the potential to reduce energy consumption by a factor. A drawback of these implementations comes from another law related to transistors, namely that the energy consumption is directly related to the execution frequency. If one performs many computations every second, the energy consumption per computation rises. Performing fewer computations lowers the energy consumption per computation. Of course, this implies that not all applications are necessarily suited for implementation using reversible circuits. However, many embedded devices do not need to perform billions of computations every second. In the rest of this section will focus on how to implement reversible gates in CMOS. First, we briefly review some basics of CMOS transistor implementation as used in this work, and afterward we explain how this is used in an implementation of reversible gates. The following are various types of reversible gates

Figure 2: Feynman gate

Figure 3: Toffoli gate

Figure 4: Peres Gate

Figure 5: Fredkin gate
The basic cell for such a multiplier is a full adder (FA) accepting three bits. We use HNG gates as reversible full adder which is depicted in Fig. 8. The proposed reversible multiplier circuit uses eight reversible HNG full adders. In addition, it needs four reversible half adders. It is possible to use HNG gate as half adder, but we use Peres gate as reversible half adder because it has less hardware complexity and quantum cost compared to the HNG gate.
4. Layout

Figure 12: Reversible multiplier and its simulation

Figure 13: Layout of Reversible multiplier

Figure 13: 250nm technology Reversible multiplier power dissipation

Figure 14: 120nm technology Reversible multiplier power dissipation
5. Implementation of Wallace tree multiplier and GCD processor:
6. RESULTS

Table 1: Comparison of foundry technologies for reversible multiplier

<table>
<thead>
<tr>
<th>Sl.No</th>
<th>Technology</th>
<th>Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>250nm</td>
<td>4.35mW</td>
</tr>
<tr>
<td>2</td>
<td>120nm</td>
<td>63.235µW</td>
</tr>
<tr>
<td>3</td>
<td>90nm</td>
<td>16.856 µW</td>
</tr>
<tr>
<td>4</td>
<td>45nm</td>
<td>1.3µW</td>
</tr>
</tbody>
</table>

Table 2: Comparative experimental results of different reversible multiplier circuits

<table>
<thead>
<tr>
<th>No. of No. of Total logical</th>
<th>No. of</th>
<th>Total logical</th>
</tr>
</thead>
<tbody>
<tr>
<td>gates</td>
<td>garbage</td>
<td>inputs/outputs</td>
</tr>
<tr>
<td>This work</td>
<td>28</td>
<td>28</td>
</tr>
<tr>
<td>[19]</td>
<td>28</td>
<td>28</td>
</tr>
<tr>
<td>[18]</td>
<td>29</td>
<td>34</td>
</tr>
<tr>
<td>[17]</td>
<td>40</td>
<td>56</td>
</tr>
</tbody>
</table>

CONCLUSION & FUTURESCOPE

From Table 1, we conclude that using 45nm the reversible multiplier is having lower dissipation. Power dissipation in multiplier designs has been much-researched in recent years, due to the importance of the multiplier circuit in a wide variety of microelectronic systems. The focus of multiplier design has traditionally been delay optimization, although this design goal has recently been supplemented by power consumption considerations. Our goal has been first to understand how power is dissipated in multipliers, and secondly to devise ways to reduce this power consumption. We have presented an investigation of multiplier power dissipation, along with some techniques which allow reductions in power consumption for this circuit. Given the importance of multipliers, it is likely that further research efforts will be directed at optimizing this block for delay and power efficiency. In this paper, we presented a novel 4x4 bit reversible multiplier circuit using HNG gates and Peres gates. Table 2 demonstrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs. Furthermore, the restrictions of reversible circuits were highly avoided. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology. All the proposed circuits are technology independent since quantum logic and optical logic implementations are not available.

REFERENCES