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Harmonic Reduction in Multilevel Inverter Using Particle Swarm Optimization

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Abstract—**In multilevel inverters, the harmonics are reduced through different types of harmonic elimination techniques, in that Selective Harmonic Elimination (SHE) technique is the most important one.. For any odd harmonics, the desired value equated to zero for the harmonics to be eliminated. Nonlinear transcendental equations are thus formed and after solving those equations, α_1 through α_k are computed.. These nonlinear equations show multiple solutions and the main difficulty is its discontinuity at certain points where no set of solution is available. This limitation is addressed by using Particle Swarm Optimization (PSO). The objective function and the constraints are formulated as the function of switching angles. The switching angles are computed by PSO algorithm. By implementing these angles as additional switching angles per quarter cycle of the output voltage waveform, the harmonics are reduced or eliminated. Two multilevel inverters (Seven level and Eleven level) are considered in this study. The THD of the output voltage is taken as the performance measure. It is found that, PSO based switching angles greatly reduces the THD when compared with the normal switching**

***Keywords*— Multilevel Inverter, Selected Harmonic Elimination (SHE), Particle Swarm Optimization (PSO), Total Harmonic Distortion (THD)**

I. INTRODUCTION

A. Multilevel Inverter

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1], [2].
Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig.1.1 shows a schematic diagram of a single phase leg of inverters

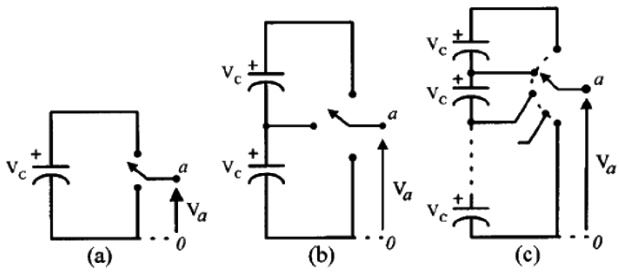

Fig1.1 Single Phase Leg of an Inverter with (a) Two levels (b) Three levels (c) n-levels with different numbers of levels,

A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1.1 (a)], while the three-level inverter generates three voltages, and so on.

B. Harmonic Elimination Technique

In multilevel inverters, there are different types techniques to reduce the voltage harmonics. Those methods are simply called as modulation strategies. The modulation methods used in multilevel inverters can be classified according to switching frequency. The methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is the space vector pulse width modulation (SVPWM) strategy, which has been used in three-level inverters. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination and the space-vector control (SVC).

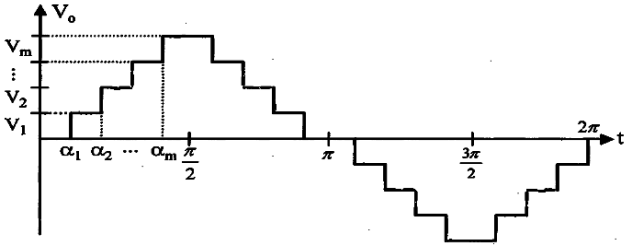

Fig 2.1 A generalized quarter-wave symmetric stepped voltage waveform synthesized by a (*2m+1*) – level inverter

TABLE I

S.No	Harmonic Elimination Techniques	Bottle Necks
1.	Traditional SHE PWM method and Carrier based PWM technique	Higher order harmonics are not completely eliminated.
2.	Active Harmonic Elimination technique and resultant theory	1) The required number of switching is high for the elimination of increased higher order harmonics. 2) At certain points of modulation indices, there are discontinuities in the solution.
3.	Theory of symmetric polynomials	1) Solutions are having discontinuity at certain points. 2) It is difficult for the controller to generate possible switching angles at those points. 3) Additional switching are required to eliminate higher order harmonics.
4.	Optimization Technique(using GA)	1)GA is struggling with premature convergence. 2)Difficulty in tuning the parameter.

II. SELECTIVE HARMONIC ELIMINATION

A generalized quarter-wave symmetric stepped voltage waveform synthesized by a (*2m+1*) – level inverter is shown in the Fig.2.12, Where '*m*' is the number of switching angles. By applying Fourier series analysis, the amplitude of any odd harmonic of the stepped waveform can be expressed as Eq.(2.12), whereas the amplitudes of all even harmonics are zero.

$$h_n = \frac{4V_k}{n\pi} \sum_{k=1}^{m} \left[\cos(n\alpha_k)\right] \qquad (2.1)$$

where V_k is the k^{th} level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and α_k switching angle. According to the Fig 2.12, α_1 to α_m must satisfy.

$$\alpha_1 < \alpha_2 < \cdots\cdots < \alpha_m < \frac{\pi}{2} \qquad (2.2)$$

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to *m*-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters [9] [10], and high-frequency harmonic components can be readily removed by using additional filter circuits. According to equation (2.12), to keep the number of eliminated harmonics at a constant level, all switching angles must be less than $\pi / 2$. However, if the switching angles do not satisfy the condition, this scheme no longer exists. As a result, this modulation strategy basically provides a narrow range of modulation index, which is its main disadvantage. For example, in a seven-level equally stepped waveform, its modulation index is only available from 0.5 to 1.05. At modulation indexes lower than 0.5, if this scheme is still applied, the allowable harmonic components to be eliminated will reduce from 2 to 1. The total harmonic distortion (THD) increases correspondingly.

III. CASCADED MULTILEVEL INVERTER

A. *Working principle*

A cascaded multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units [11] [12] [7] [14] [15]. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCS's), which may be obtained from batteries, fuel cells, or solar cells. Fig.3.1 shows a single-phase structure of a cascade inverter with SDCS's. Each SDCS is connected to a single-phase full bridge inverter. Each inverter level can generate three different Voltage outputs, $+V_{dc}$, *0*, and $-V_{dc}$, by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain *+Vdc*, switches S_1 and S_4 are turned on. Turning on switches S_2 and S_3 yields $-V_{dc}$. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is zero. The ac outputs of each of the different level full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascade inverter is defined by '*m = 2s+1*', where's' is the number of dc sources. An example phase voltage waveform for an 11-level cascaded inverter with five SDSC's and five full bridges is shown in Fig.3.2.

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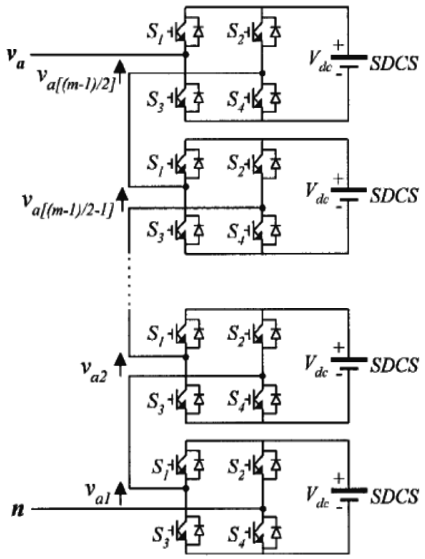


Fig 3.1 Single Phase Structure of a Multilevel Cascaded Inverter

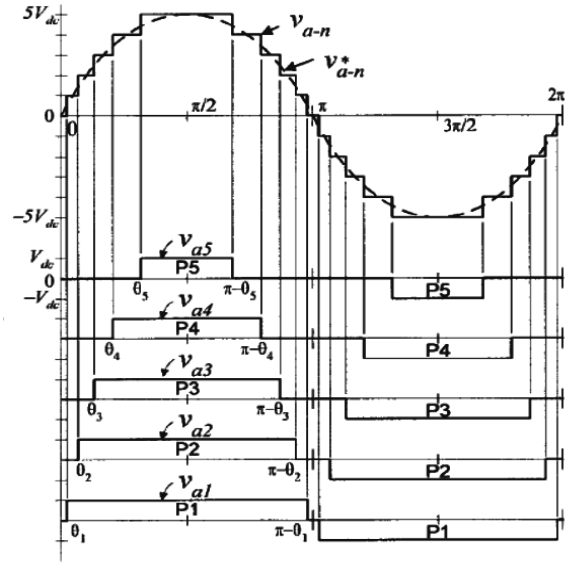


Fig 3.2 Output Voltage Waveform of the 11 Level Cascade Inverter.

The phase voltage '*Van*' of the waveform which is shown in Fig.3.2 is expressed as

$$V_{an} = V_{a1} + V_{a2} + V_{a3} + V_{a4} + V_{a5} \quad (3.1)$$

The output voltage of the inverter is almost sinusoidal, and it has less than 5% THD with each of the bridges switching only at fundamental frequency. Each bridge unit generates a quasi – square waveform by phase shifting its positive and negative phase legs switching timings. The Fig.3.3 shows the switching timings to generate a quasi sine waveform. Note that each switching device always conducts for 180° (or ½ cycles), regardless of the pulse width of the quasi – square wave. This switching method makes all of the active devices current stress equal. For a stepped waveform such as the one depicted in Fig.3.2 with '*s*' steps, the Fourier Trans- form for this waveform is as follows:

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)] \times \frac{\sin(n\omega t)}{n}$$

Where, n = 1, 2, 3, 7, (3.2)

$$H(n) = \frac{4}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]$$

Where, n = 1, 2, 3, 5, 7, (3.3)

The conduction angles θ_1, θ_2,……,θ_s can be chosen such that the voltage total harmonic distortion is a minimum. Normally these angles are chosen so as to cancel the predominant lower frequency harmonics.

B. Features

For real power conversions, (ac to dc and dc to ac), the Cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc. Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously. The main advantages are, it requires the least number of components among all multilevel converters to achieve the same number of voltage levels and the soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers. The main disadvantage is, it needs separate dc sources for real power conversions, and thus it applications are somewhat limited.

IV. PARTICLE SWARM OPTIMIZATION

Particle Swarm Optimization is similar to genetic algorithm in that system is initialized with a population of random solutions. It is unlike a GA, however, in that each potential solution is also assigned a randomized velocity, and then "flown" through the hyperspace.

1) Each particle keeps track of its coordinates in hyperspace which are associated with the best solution (fitness). This value is called pbest.
2) The "global" version of the particle swarm optimizer keep track of the overall best value, and its location, obtained thus far by any particle in the population, this is called gbest.

3) The PSO concept consists, at each time step, changing the velocity (accelerating) each particle toward its pbest and gbest.
4) Acceleration is weighted by a random term, with separate random numbers being generated for acceleration toward pbest and gbest.

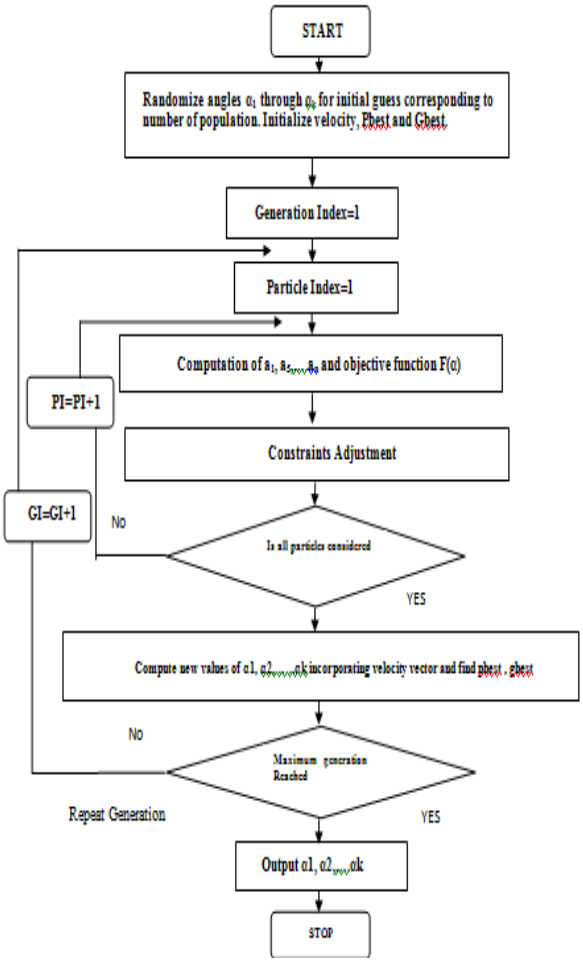


Fig 4.1 Flow Chart for PSO Algorithm

V. SIMULATION RESULTS AND ANALYSIS

To reduce the harmonics, the switching angles are computed by the PSO technique and the switching angles are used as additional switchings along with the fundamental switching. Six switchings are added per quarter cycle and the output voltage is shown in Fig 5.1 below.

The switching angles are: α_1= 20.241, α_2= 45.78318, α_3= 71.80722.

The frequency spectrum of the output voltage waveform obtain with additional switching angles is shown in Fig 5.2. It is clear that the magnitude of the 7th and 11th order harmonics are reduced. The 3rd order harmonic can be eliminated by suitable transformer connection.

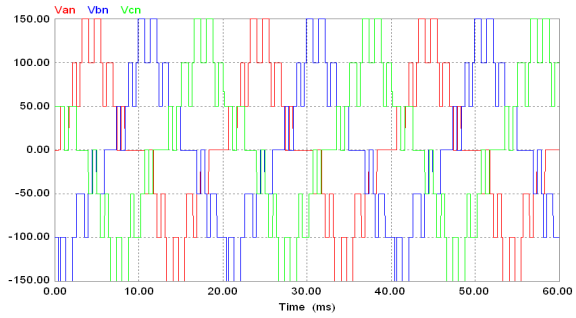


Fig 5.1 Three Phase Output Voltage Waveform of Seven Level Cascaded Multilevel Inverter using additional switching

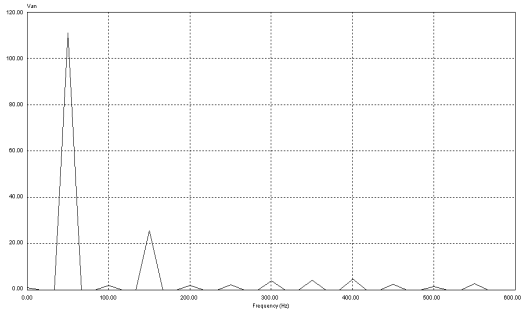


Fig 5.2 FFT Analysis of Seven Level Cascaded Multilevel Inverter using Additional Switching

The THD level of the seven level inverter with additional switching is shown in Fig.5.3 and the THD value is reduced to 0.4%.

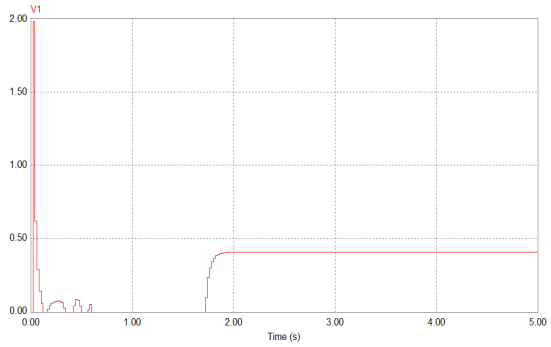


Fig 5.3 THD of Seven Level Cascaded Multilevel Inverter using Additional Switching

To reduce the harmonics, the switching angles are computed by the PSO technique and the switching angles are used as additional switchings along with the fundamental switching. Eight switchings are added per quarter cycle and the output voltage is shown in Fig 5.4 below.

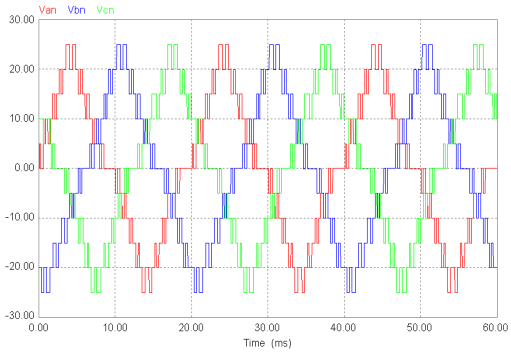


Fig 5.4 Three Phase Output Voltage Waveform of Eleven Level Cascaded Multilevel Inverter using additional switching

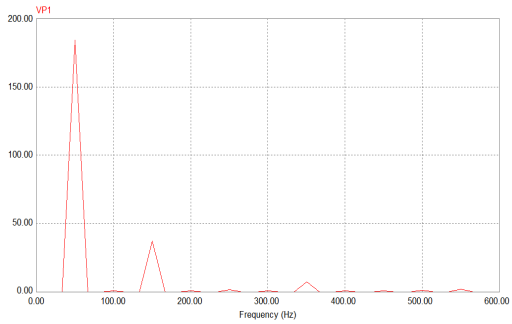
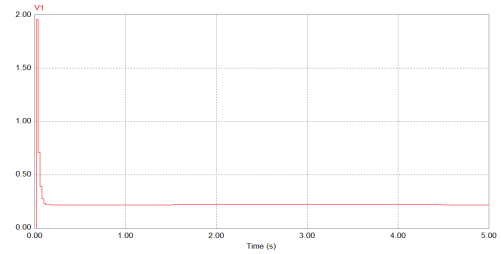


Fig 5.5 FFT Analysis of Eleven Level Cascaded Multilevel Inverter using Additional Switching

The THD level of the seven level inverter with additional switching is shown in Fig.5.6 and the THD value is reduced to 0.2%.



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ig 5.6 THD of Eleven Level Cascaded Multilevel Inverter using Additional Switching

The switching angles are: α_1= 32.2253, α_2= 45.5120, α_3= 57.8096, α_4=72.0000, α_5=88.5145.

The frequency spectrum of the output voltage waveform obtain with additional switching angles is shown in Fig 5.5. It is clear that the magnitude of the 5^{th} , 7^{th} and 11^{th} order harmonics are reduced. The 3^{rd} order harmonic can be eliminated by suitable transformer connection.

VI. Conclusions

Harmonics are always present in a multilevel inverter. These harmonics can be eliminated by the proper selection of switching angles. Particle Swarm Optimization technique (PSO) is proposed to minimize the overall THD of the output voltage of a multilevel inverter. While computing the switching angles with the help of developed algorithm, all the multiple solutions are found wherever exists. The additional switching is used to eliminate the selected higher order harmonics along with the lower order harmonics. The THD value of the multilevel inverter with fundamental switching is 0.8% and then the THD is reduced to 0.4% by additional switching for seven level CMI. For eleven level the THD value of the multilevel inverter with fundamental switching is 0.35% and then the THD is reduced to 0.2% by additional switching. The proposed scheme can be efficiently employed for the control of multilevel inverter supplied from different dc sources.

VII. References

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