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Implementation of BCD Adder using Clockgating

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Abstract

There is a growing importance of decimal arithmetic in commercial, financial and internet based applications. These applications cannot tolerate errors that result from the conversion of binary format to decimal format. Thus, hardware support for decimal arithmetic is receiving considerable attention.BCD adder are used for such applications. Clock gating is a power reduction technique that has been used successfully in the custom ASIC domain. Clock and logic signal power are saved by temporarily disabling the clock signal on registers whose outputs do not affect circuit outputs. Clock gating is a way of reducing switching activity on circuit signals, and it entails temporarily disabling the clocking of specific registers when the outputs of those registers are inconsequential to circuit outputs. In this paper implementation of BCD adder using VHDL is done. Clock Gating technique is applied to the designed BCD adder, Comparison of power dissipated with and without clock gating is done. Dynamic Power, Static power are affected in this design. VHDL language is used to implement the BCD adder. Mimas V2 Spartan 6 FPGA Development Board is used.

Keywords: *BCD Adder, Power Dissipation, ClockGating,VHDL.*

1. Introduction

In digital design, One of the important issue for VLSI designers is Power consumption. For battery-operated systems, such as laptops, calculators, cell phones and MP3 players power dissipation is critical since it determines the battery life and has a direct impact on the consumer valuation of the product. Obtaining Low power consumption is primary requirement in todays design. Power consumption in CMOS circuits can be divided in two components, Static dissipation, which is due to leakage current. Leakage current is a small current that flows through the transistor even when the transistor is off and there is no switching activity. Dynamic dissipation, which is due to charging and discharging of load capacitances and short circuit currents while both pMOs and nMOS networks are partially on. Total Power, Dynamic power, Static Power are given by

$P_{total}=P_{Dynamic}+P_{Static}$----------(1) $P_{Dynamic}=1/2\ \alpha CfV^2$----------(2) where C is Load Capacitance, f is frequency, Supply Voltage. α is activity factor. $P_{static}= V_{cc}I_{cc}$---------- (3)

With BCD Adder Decimal addition is possible. The decimal sum of the addend and augend, and a carry that is generated if the sum exceeds a decimal value of 9 is produced. As the IEEE standard for decimal floating point is approved, hardware support for decimal floating point arithmetic will be incorporated in processors for various applications. Still, a major consideration while implementing Binary Coded Decimal (BCD) arithmetic is to enhance its speed as much as possible. BCD is a decimal representation of a number directly coded in binary, digit by digit. For example, the number $(9527)_{10}$ is represented as (1001 0101 0010 0111) BCD . It can be seen that each digit of the decimal number is coded in binary and then concatenated to form BCD representation of the decimal number. To use this representation all the arithmetic and logical operations need to be defined. As the decimal number system contains 10 digits, at least 4 bits are needed to represent a BCD digit. Addition in BCD can be explained by considering two decimal digits A and B with BCD representations as A4A3A2A1 and B4B3B2B1 respectively. In the conventional approach, these two numbers are added using a 4-bit binary adder during which it is possible that the resultant Sum can exceed 9 resulting in an overflow. If the Sum is greater than 9, the binary equivalent of 6 is added to the resultant Sum to obtain the exact BCD representation.

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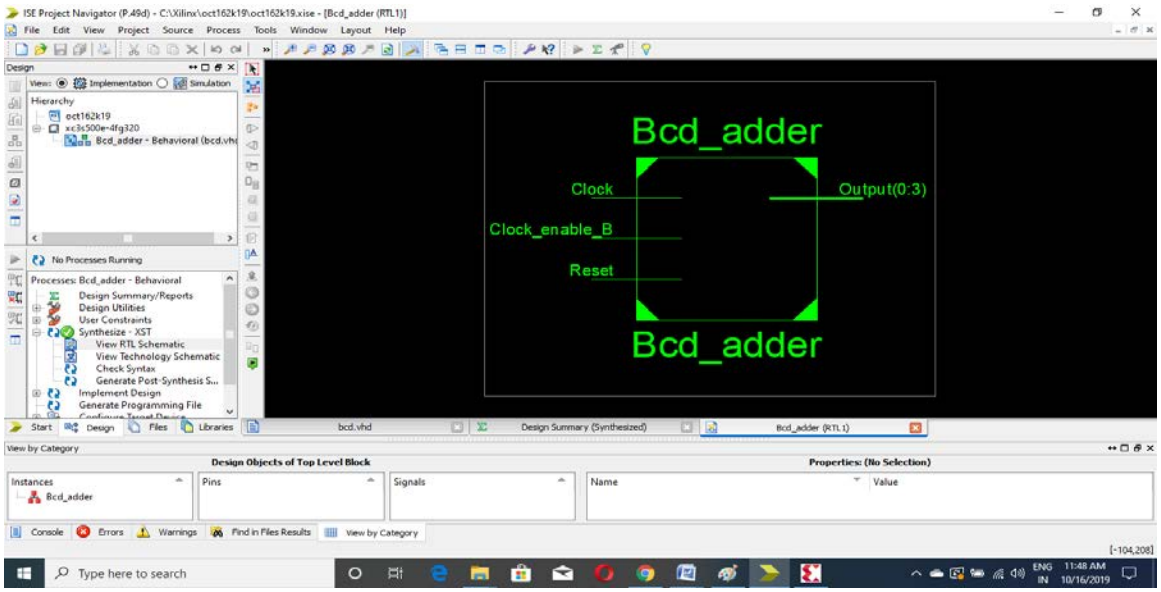
2. Clock Gating

Gate based clock gating are of two types AND, NOR based. The AND gate is the most common gate used for clock gating because of its simple logic. To gate the clock, a two input AND gate is inserted in the four bit counter having one of its input as clock and other as the enable signal “En”. When enable signal is equal to zero and the clock can take any value (i.e. it can either be in positive or negative cycle). The output of the AND gate which is also known as the gated clock “GCLK = 0”. When enable is equal to one then the output of the gated clock (GCLK) varies according to the clock signal. When output of the gated clock (GCLK) undergoes a transition from high to low (i.e. when the negative edge occurs), the counter gets incremented. The drawback in this technique is that, for the positive edge triggered counter when enable signal goes from 1 to 0 and when the clock is at rising edge, a glitch occurs because of the greater falling time period of enable signal. The output obtained is incorrect, because of the aforementioned reason. Any hazard that occurs when enable is equal to one is directly imprinted on to the GCLK this is an unstable behavior of the circuit. The NOR gate gives output of the gated clock (GCLK) equal to one only when both enable and the clock have a value zero. Hence the enable signal is passed through a NOT gate before being fed as one of the inputs of the NOR gate so that the output of the gated clock (GCLK) is obtained when enable is ON. NOR gate clock gating is used in particular for positive edge triggered circuits.

3. Implementation

Implementation of BCD adder without and with clock gating is done using VHDL. Below figure represents the respective Schematic and Device Utilization summary.



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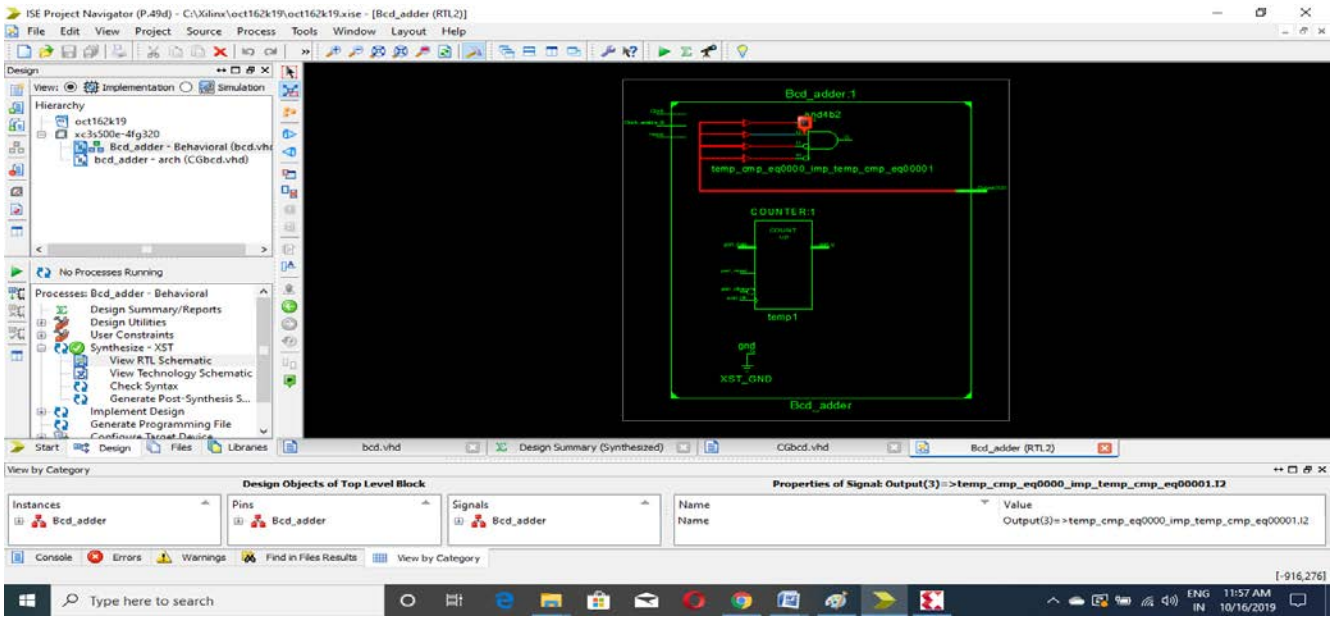


Fig. 1. Schematic view of BCD adder

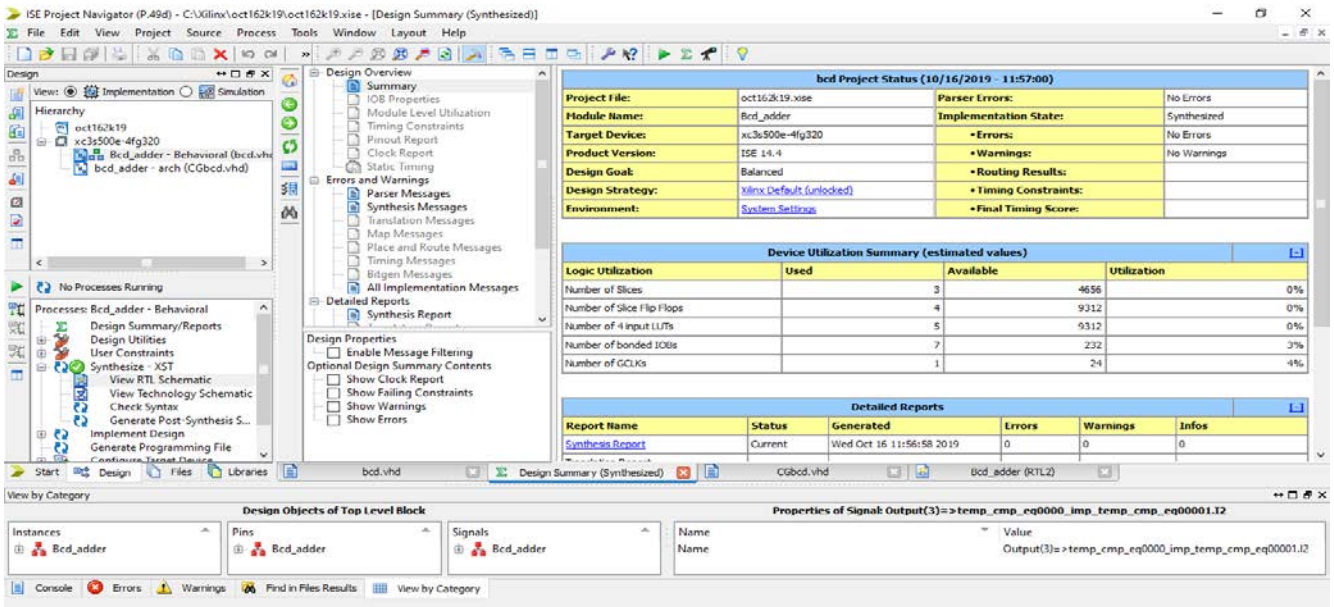
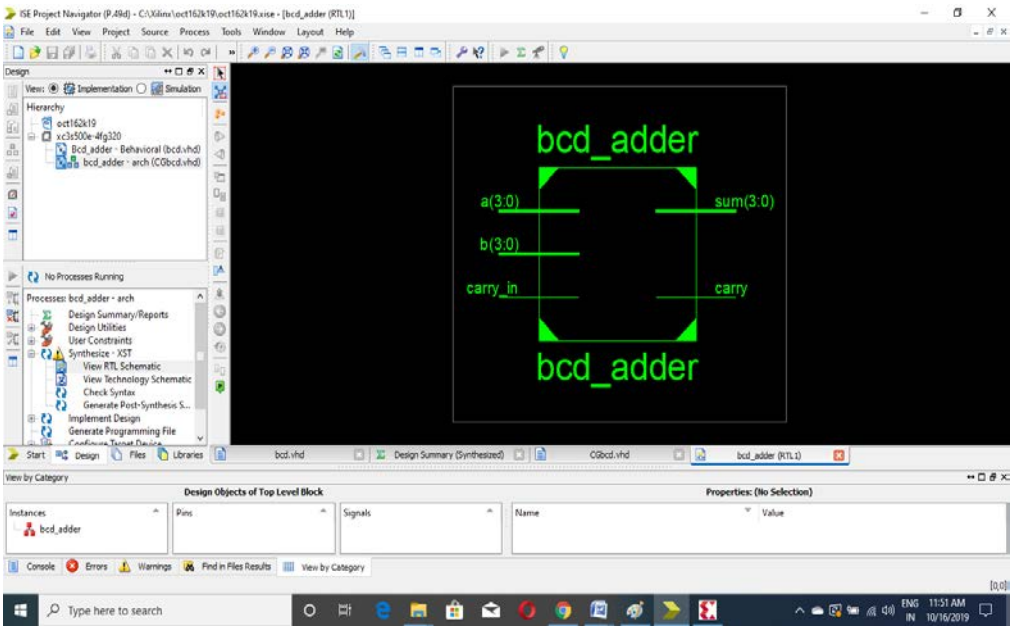


Fig. 2. Device Utilization of BCD adder

In the device utilization summary no of IOB's, GCLK's is 3% and 4% respectively.



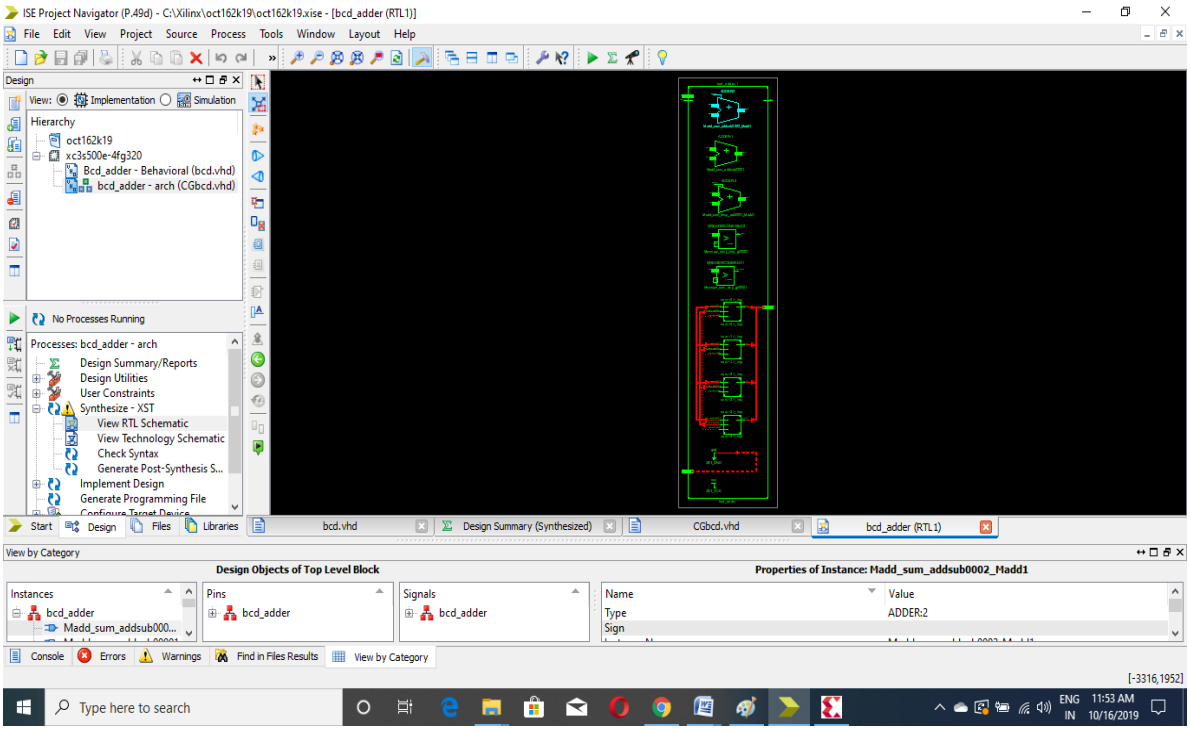


Fig. 3. Schematic of 4 bit BCD adder

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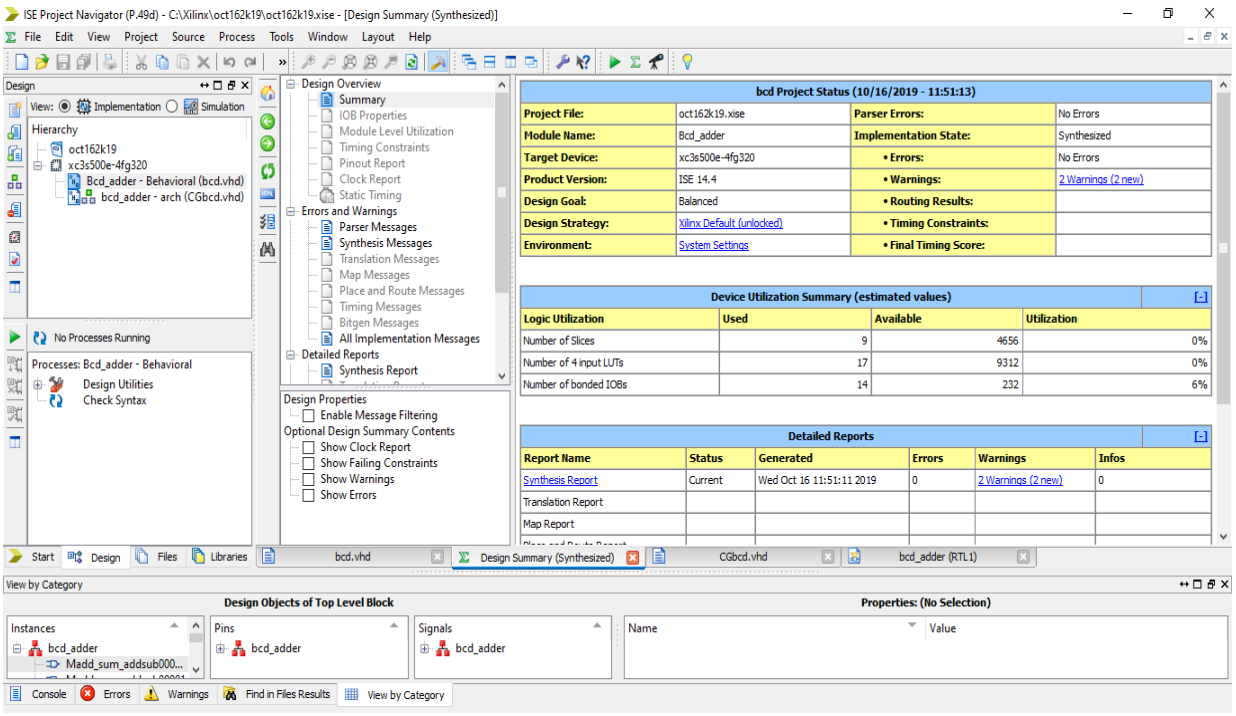

Fig. 4. Device Utilization of 4 bit BCD adder

In the device utilization summary of 4-bit BCD adder, no of IOB's, is 6% , when compared with nonclockgating BCD adder.

4. Conclusions

Without clock gating results are

Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	14.11	0.45	13.66

With Clock gating results are

Power Supply Summary

Power Supply Summary			
	Total	Dynamic	Static Power
Supply Power (mW)	13.65	0.00	13.65

From the above results it is clear that the BCD adder with Clock gating is dissipating less power when compared with normal clock. The total power which is a combination of static and dynamic power is affected with 3.189 %. Therefore we can conclude that dynamic power is affected by clock gating technique. Future work will involve incorporating the clock gating aware placement algorithm into a complete power-aware FPGA CAD flow, allowing trade-offs between other power-aware tool phases to be explored. Another future direction involves modeling clock gating within the VPR router to permit extraction of accurate post-routing critical path delay and interconnect capacitance. It will also be important to understand the impact of gating on timing analysis to ensure functional correctness is maintained when enable signals are migrated from flip-flops to enable pins on clock network switches.

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