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Novel Low Power, High Gain, Operational Amplifier

Srikar Datta Canchi, Gande Bhargav, Govind Prasad

Integrated Dual Degree (B-Tech + M-Tech (VLSI Design))
GITAM University, Hyderabad campus,

Abstract: In today's low power environment, to design a high gain and low power operational amplifier is a challenge to the designer. The design of an amplifier with robust nature and with sustaining the conventional nature of amplifier is the need of the hour. The proposed circuit here tries to produce a very low power and considerably good gain operational amplifier for low frequency applications. In low power design here, we have implemented various conventional and modern low power techniques and maintaining the gain to the optimum level. Body-bias technique is the important low power tool implemented here in accordance with the proposed 'Rail sensing circuit', which not only reduces the static power consumption but is utilized for it self-biasing mechanism in the amplifier. Conventional low power technique of 'stack transistors' is utilized for reducing the power effectively. The effects of these techniques have been analyzed and presented. The design has been implemented in a 0.25 µm technology in TANNER EDA V 15.0 tool with V_{dd} of 3 v. The proposed work has voltage Gain of 68.45 dB and with the total power of 28 µW with operating frequency of 875 KHz and bandwidth of 350 Hz.

Keywords- Differential Amplifier, High Gain, Low Power Analog Circuits, Single Ended Amplifier, MOSFET Amplifier, Two Stage Amplifier.

I. INTRODUCTION

Today in the world of complete portability, there is a certain need of minimizing the sizes of gadgets carried without compromising their workability. This need brings us to various low power design methods, one of it is reducing the power consumption through the supply. These low power design methodologies focuses the areas of reducing the usage of the power in various stages of operation of general gadgets like reducing usage of power in 'standby mode', 'hibernation mode', 'sleep mode' and various stages in which the gadget is operated, like reducing the usage of power in the components itself without any trade-off in performance.

Operational amplifier (Op-amp) is the basic building block of analog circuits. Various applications are derived using the Op-amp. These applications include the use of Op-amp as comparator, integrator, differentiator, audio amplifier and much more. The op-amp is a type of differential amplifier which include the fully differential amplifier, the instrumentation amplifier. The classic model of the voltage feedback op amp incorporates the following characteristics: [1]

- Infinite input impedance.
- Infinite bandwidth.
- Infinite gain.
- Zero output impedance.
- Zero power consumption.

The important quality of Op-amp is the voltage gain which is also known as open-loop gain (usually referred to as AVOL) which is the gain of the amplifier without the feedback loop being closed, hence the name "open-loop." For a precision op amp this gain can be very high, on the order of 160 dB. This is a gain of 10^8. This gain is flat from dc referred to as the dominant pole. From there it falls off at 20 dB/decade. This is referred as a single-pole response. It will continue to fall at this rate until it hits another pole in the response. This 2nd pole will double the rate at which the open-loop gain falls, that is, to 40 dB/decade. If the open-loop gain has dropped below 0 dB (unity gain) before it hits the 2nd pole, the op amp will be unconditional stable at any gain. This will be typically referred to as unity gain stable. If the 2nd pole is reached while the loop gain is greater than 1 (0 dB), then the amplifier may not be stable under some conditions. [1]

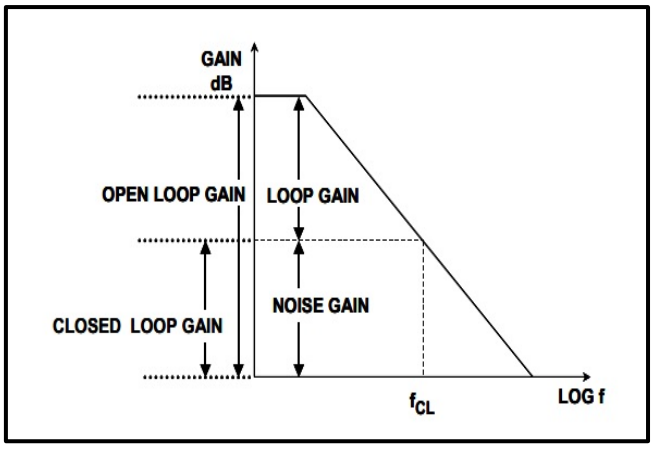

Fig 1: Gain definition

The open-loop gain falls at 20 dB/decade. This means that if we double the frequency, the gain falls to half of what it was. Conversely,

If the frequency is halved, the open-loop gain will double, as shown in above Figure.

This gives rise to what is known as the Gain-Bandwidth Product. The product of the open-loop gain to the frequency the product is always a constant. The caveat for this is that we have to be in the part of the curve that is falling at 20 dB/decade. This gives us a convenient figure of merit with which to determine if a particular op amp is useable in a particular application. [1]

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II. OP-AMP DESIGN

An operational amplifier is an input signal amplifier which is derived from differential amplifier (high input impedance amplifier stage), a voltage gain amplifier, a level shifter and a unity gain buffer.

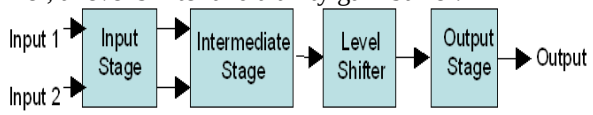

Fig 2: Basic block diagram of an op-amp [15]

Upon a close look of the conventional operational amplifier circuit given below, we shall find that it consists of an active current load, differential amplifier, current mirror and common source amplifier as the second stage. The active current load and current mirror is used to bias the circuit. Here we have two current mirrors, one acts as an active current load and another acts as a current mirror. These are employed for maximum current flow in the circuit. The differential amplifier here is a two stage, single ended type voltage amplifier. The second stage is common source stage is used for high swing. The high gain and high swing is necessary for a near ideal op-amp design

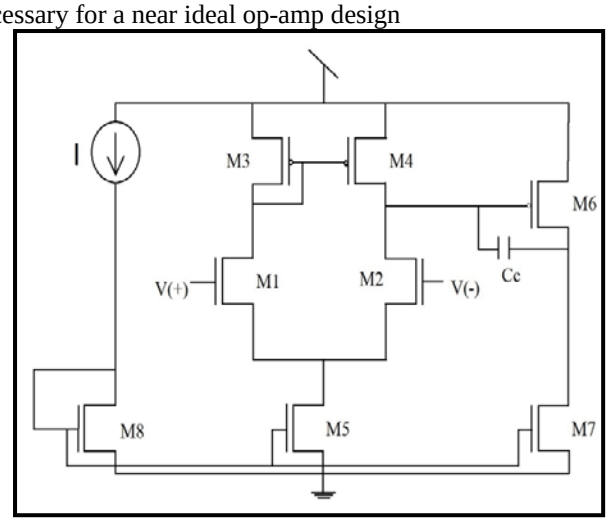

Fig 3: Conventional Op-amp

In the above figure transistors M8 and M5 will reduce the fluctuations in current and give constant current for driving. Transistors M7 and M6 will comprise to a common source which will increase the gain of the first stage. The capacitor C_c is used as the miller capacitance.

Designing of the circuit can be done by the following set of expressions: First we derive the load capacitance and coupled capacitance values:

$$C_C = .22C_L \quad (1)$$

Then the current through them are calculated:

$$I_5 = SR * C_C \quad (2)$$

The $\frac{W}{L}$ ratio is calculated which is important for the design, where L is the technology, here it is 250nm and W is the width of the transistor used. So we calculate the widths and lengths of all the transistors using the equation below1:

$$\left(\frac{W}{L}\right)_3 \equiv \frac{I_5}{K_3[(V_{DD} - V_{in(\max)}) - V_{t3(\max)} + V_{t1(\min)}]^2} \quad (3)$$

Trans-conductance is calculated using the coupled capacitance and unity gain bandwidth (UGB):

$$g_{m1} = UGB * C_C * 2\Pi \quad (4)$$

The $\frac{W}{L}$ ratios of two transistors are compared namely M1 and M2. Then we get the ratio of square of transconductance of first transistor and current calculated in eq. (2).

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{m1}^{\ 2}}{I_5 k_3} \quad (5)$$

Drain to source voltage is calculated with the difference of minimum input voltage ($V_{in(\min)}$), source voltage and minimum threshold voltage.

$$V_{DSS} = V_{in(\min)} - V_{ss} - \sqrt{\frac{I_5}{\beta_1}} - V_{t1(\min)} \quad (6)$$

With the help of the current through the 5th transistor we can find the size of the transistor.

$$\left(\frac{W}{L}\right)_5 = \frac{2.I_5}{K_n (V_{DSS})^2} \quad (7)$$

In order to obtain the good phase margin the below condition should be considered.

$$g_{m6} = 10 g_{m1} \quad (8)$$

We know that the ratio of the transistor sizes is directly proportional to the ratio of the transconductance, then.

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{g_{m4}} \left(\frac{W}{L}\right)_4 \quad (9)$$

Now we can find the current through the 6th transistor as.

$$I_6 = \frac{g_{m6}^{\ 2}}{2K_6 S_5} \quad (10)$$

As current through the transistor is proportional to the transconductance above discussed equation can be modifies as.

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5} \left(\frac{W}{L}\right)_5 \quad (11)$$

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All transistors are designed such that they operate in saturation region. All device dimensions are tabled in table1.

TABLE I. SPECIFICATIONS OF TRANSISTORS

Transistors	Aspect Ratios	Region of operation
M1,M2	3	Saturation
M3,M4	30	Saturation
M5,M9	6	Saturation
M6	194	Saturation
M7	20	Saturation
M8	12	Saturation

The second stage is a current sink load inverter. It takes output from stage 1 and amplifies it through M6. Here buffer stage is eliminated, so this is called as the transconductance amplifier.

Here the differential amplifier is in single ended output mode, which is fed to transistor M6. As we have used single ended mode so we have an active current load on the top. A single-ended system is a system with a single output referred to the common terminal (ground).

We design the op-amp in 250nm technology using tanner tool. Here we consider supply voltage as 3V. Simulation of this circuit is done in Tanner EDA v15 to obtain the responses. Here with the help of AC response we obtain magnitude and frequency response, power is obtained by using the transient analysis. Plots for various responses are:

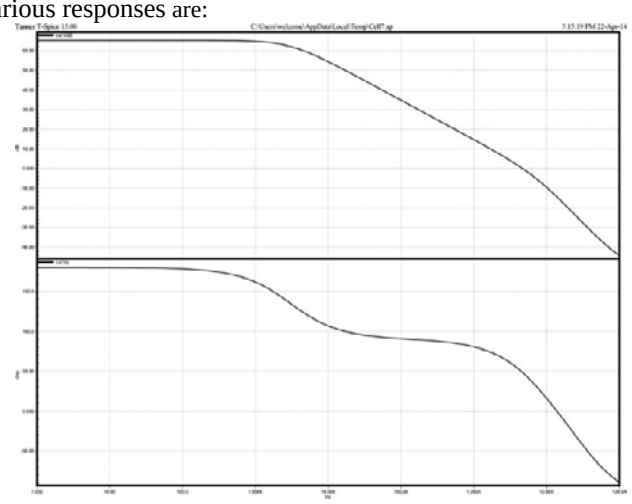

Fig 4: Gain and Phase plot of Conventional Op-amp

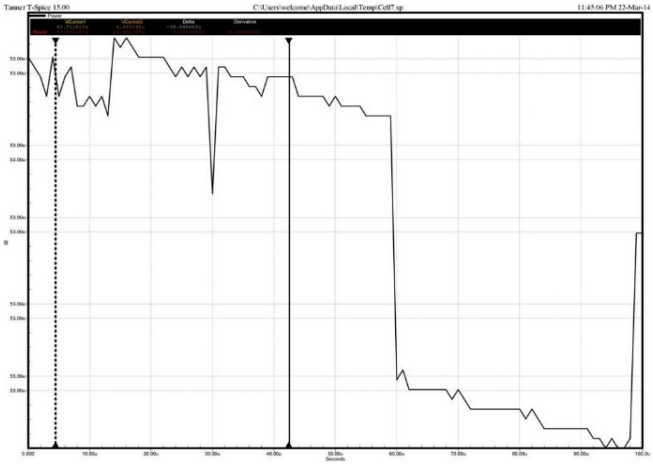

Fig 5: Power plot of Conventional Op-amp

III. PROPOSED DESIGN

The circuit so far designed and discussed is the conventional operational amplifier. In our proposed design we have employed two methods which reduce power consumption and increase the gain, namely stacking of transistors and body biasing techniques.

A. Stacking Effect:

We know that sub threshold current of a MOSFET will depend exponentially on V_t, V_{gs}, V_{ds} and hence on the terminal voltages. This is shown in the below equation.

$$I_D = \frac{W}{L} I_{D0} e^{\left(\frac{V_{GS}}{nkt/q}\right)} \quad (12)$$

So by controlling the terminal voltages the sub threshold leakage can be controlled. This technique is used here.

B. Body bias:

We can alter the threshold voltage of the transistors by varying few parameters. Threshold voltage of the transistors can be varied with the body voltage. The relationship between threshold-voltage and VBS which is called bulk bias voltage, is given as:

$$V_t = V_{th0} + \gamma\left(\sqrt{2\phi_F + VBS} - \sqrt{2\varphi_F}\right) \quad (13)$$

Now by using these techniques we can reduce the power consumed by the op-amp and at the same time without much effecting the other parameters. The proposed circuit is as follows:

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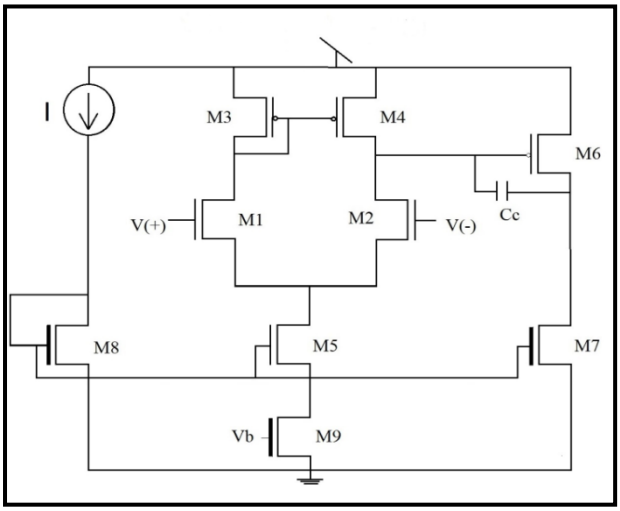

Fig 6: Proposed op-amp design

The simulation results of the proposed circuit can be shown as:

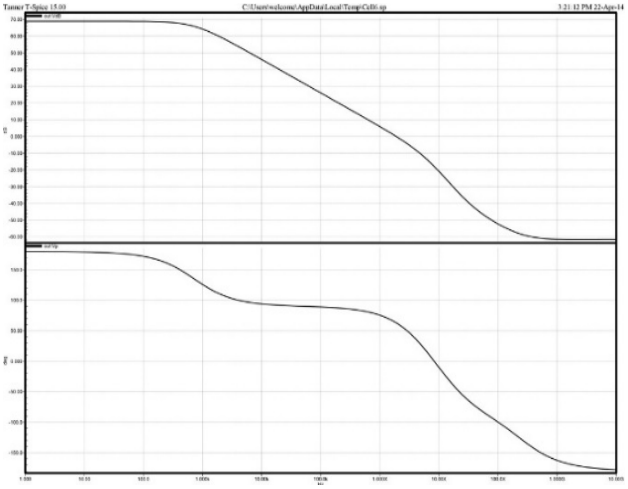

Fig 7: Gain and Phase plot of proposed op-amp design

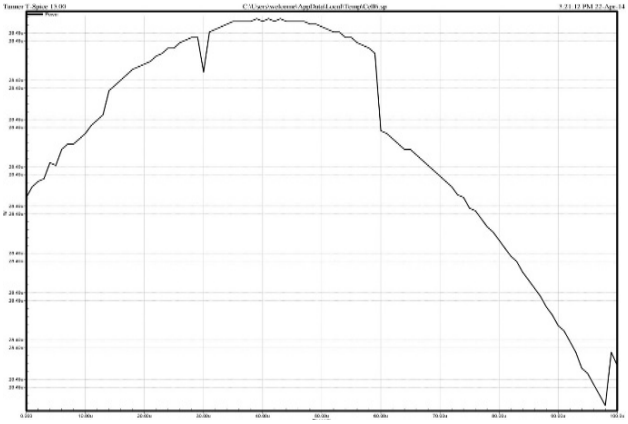

Fig 8: Power plot of proposed op-amp design

From these plots the calculated parameter values are tabled as

TABLE II. PERFORMANCE TABLE

Specifications	Conventional	Proposed
Gain	65.46 db	68.85
Phase margin	58	64
Power	53.09uW	28.49uW
Band width	1.45KHz	335Hz
Gain Bandwidth frequency	2.28MHz	875KHz

From the table 2 we can clearly observe that the power is reduced by 46.33%

IV. CONCLUSION

The proposed op-amp showed improvements in all the parameters than the conventional design of op-amp which is implemented in 0.25 µm with V_{DD} 3V. The proposed design has been able to satisfy most of the specifications provided for the op-amp. The proposed op-amp is a two stage single ended output op-amp. The input stage is a differential amplifier and a common source stage forms the second stage of the op-amp. The SPICE design has been made and simulated. The pre layout simulations abide by the given specification. The entire design has been done in UMC 250 nm technology Tanner EDA version 15.

V. ACKNOWLEDGEMENT

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