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Design of Digit Serial FIR Filter Using VHDL

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Abstract

In the last two decades, many efficient algorithms and architectures have been introduced for the design of low complexity bit-parallel multiple constant multiplications (MCM) operation which dominates the complexity of many digital signal processing systems. On the other hand, little attention has been given to the digit-serial MCM design that offers alternative low complexity MCM operations albeit at the cost of an increased delay. In this paper, we address the problem of optimizing the gate-level area in digit-serial MCM designs and introduce high-level synthesis algorithms, design architectures, and a computer aided design tool. Experimental results show the efficiency of the proposed optimization algorithms and of the digit-serial MCM architectures in the design of digit-serial MCM operations and finite impulse response filters.

1. Introduction

Finite impulse response (FIR) filters are widely used in digital signal processing applications due to their stability and linear phase characteristics. FIR filters have a large number of multiplications involved in the filter algorithm, which are usually implemented using fixed-point or integer number representations with the filter coefficients being represented by a finite number of bits. In hard-wired ASIC designs, multiplication operations are replaced by shift-and-add operations towards multiplier less FIR filter design. From a power perspective, the fewer the number of adders, the less power the filter will consume.

The most common approaches to the implementation of digital filtering algorithms are general purpose digital signal processing chips for audio applications, or special purpose digital filtering chips and application-specific integrated circuits (ASICs) for higher rates. This project describes an approach to the implementation of digital filter algorithms on field programmable gate arrays (FPGAs). Recent advances in FPGA technology have enabled these devices to be applied to a variety of applications traditionally reserved for ASICs. FPGAs are well suited to data path designs, such as those encountered in digital filtering applications. The density of the new programmable devices is such that a nontrivial number of arithmetic operations such as those encountered in digital filtering may be implemented on a single device. The advantages of the FPGA approach to digital filter implementation include higher sampling rates than are available from traditional DSP chips, lower costs than an ASIC for moderate volume applications, and more flexibility than the alternate approaches.

In particular, multiple multiply-accumulate (MAC) units may be implemented on a single FPGA, which provides comparable performance to general-purpose architectures which have a single MAC unit.

In the majority of digital signal processing (DSP) applications the critical operations are the multiplication and accumulation. Real-time signal processing requires high speed and high throughput Multiplier-Accumulator (MAC) unit that consumes low power, which is always a key to achieve a high performance digital signal processing system. The purpose of this work is, design and implementation of a low power MAC unit with block enabling technique to save power.

2. Filter Design

In direct form structure even though there are only two multipliers, there are still three delays (same as for the direct-form structure) required since the number of delays corresponds to the order of the filter.

The direct-form structure has the disadvantage that each adder has to wait for the previous adder to finish before it can compute its result. For high speed hardware such as FPGAs/ASICs, this introduces latency which limits how fast the filter can be clocked.

A solution to this is to use the transposed direct-form structure instead. With this structure, the delays between the adders can be used for pipelining purposes and therefore all additions/multiplications can be

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performed in fully parallel fashion. This allows real-time handling of data with very high sampling frequencies.

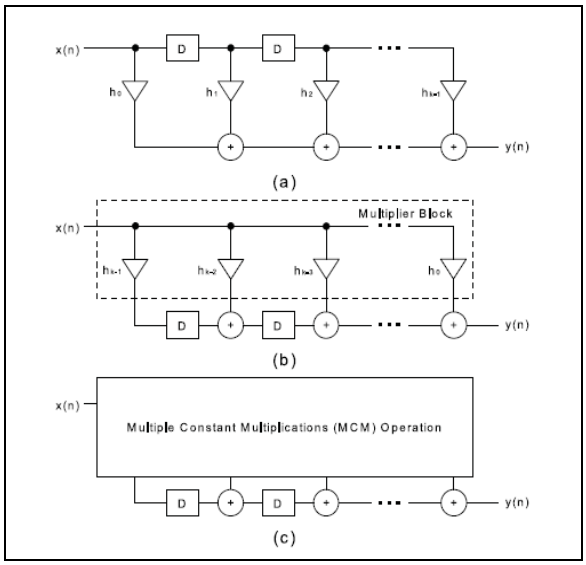

Fig 1 FIR filters implementations. (a) Direct form. (b) Transposed form with generic multipliers. (c) Transposed form with an MCM block.

2.1Coefficient Verification through Mat lab

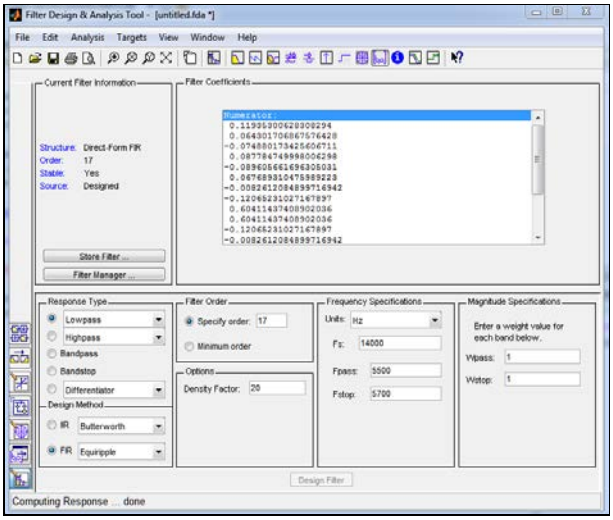

Fig 2

Whatever the coefficients of fir filter are obtained by MATLAB, we face the following problems:

1. Floating point coefficients.
2. Negative coefficients.

2.2 Direct Form Structure

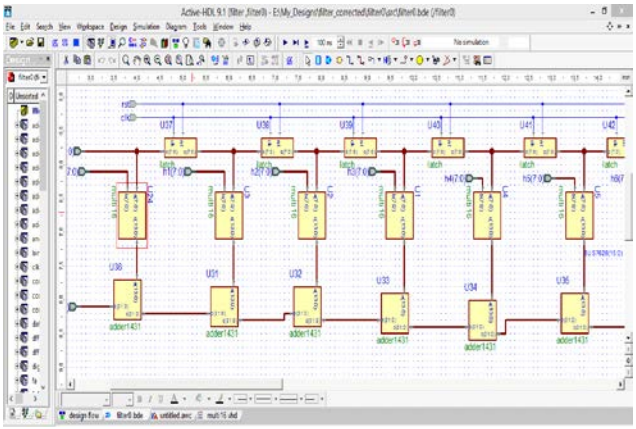

Fig 3

Fig 3 shows the direct form 18 tap FIR filter in which adder unit ,multiplier unit and latch are connected with reset and clock pulse as it is the direct form filter with rst and clock in which every adder circuit operates until the previous stage is free so required more time in this circuit hence transpose form structure . In the direct form structure the latch is connected in input side.

2.3 Transpose Form Structure

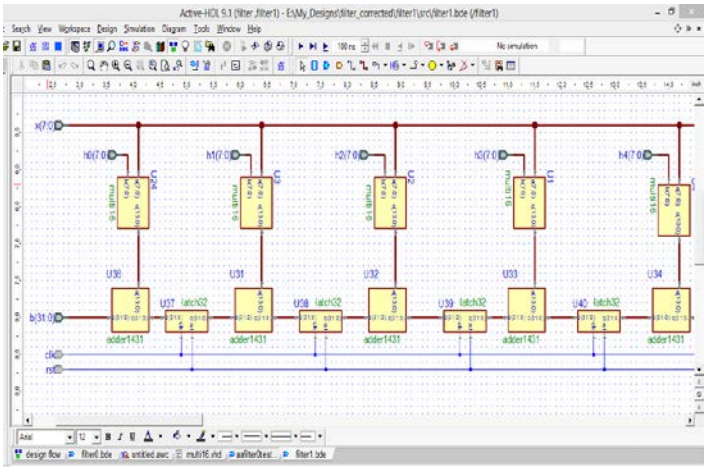

Fig 4

Fig 4 shows the transpose form 18 tap FIR filter in which adder unit ,multiplier unit and latch are connected with reset and clock pulse but it is in transpose form With this structure, the delays between the adders can be used for pipelining purposes and therefore all

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additions/multiplications can be performed in fully parallel fashion. Latches are connected in the output side so that it operates in less time duration. Wave form for such a direct and transpose form are shown below.

2.4Output Clock Pulses of direct & transpose form

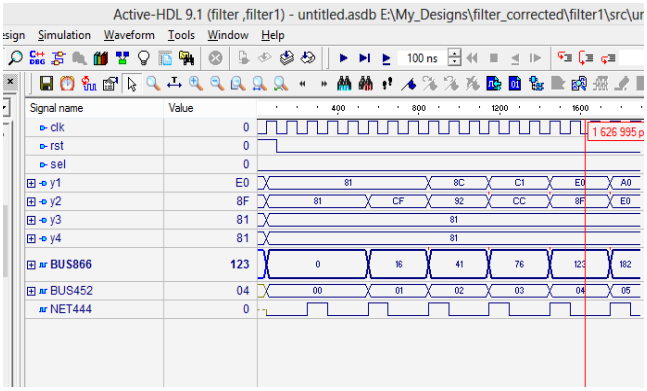


Fig 5

2.5 Optimized Structure

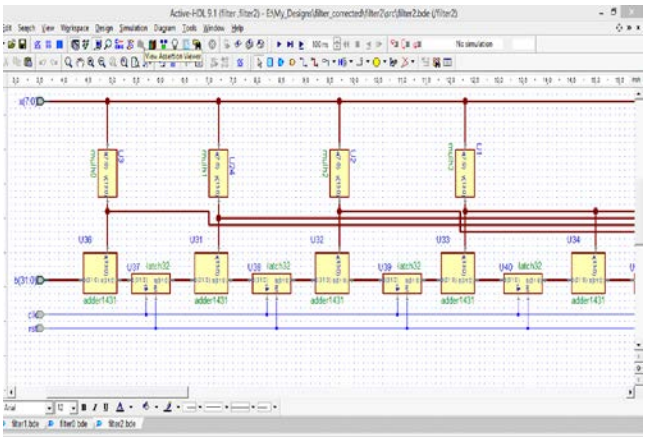


Fig 5 Optimized Form of FIR filter using Active HDL

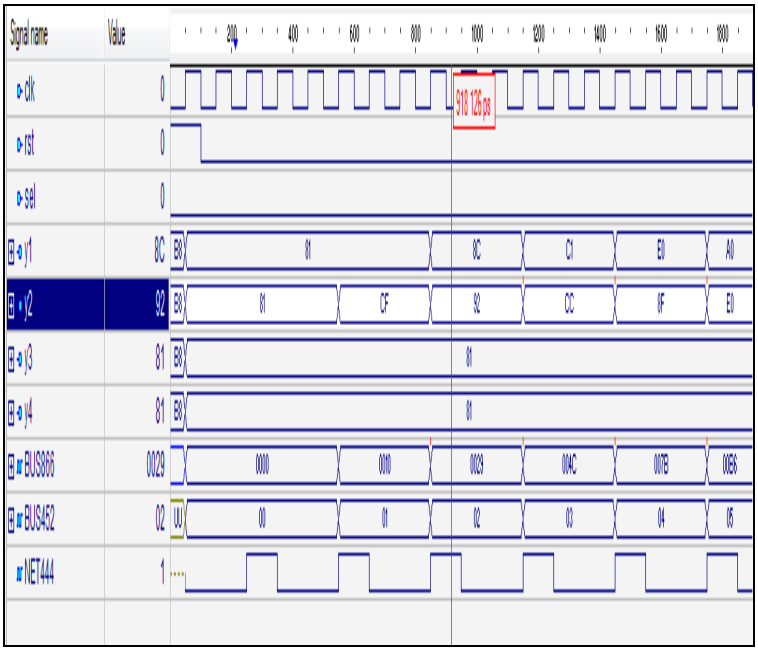
Fig 5 shows the optimized form of FIR filter as in this optimized form circuit is similar in design to that of transpose structure but only the MAC unit is used ,here also the clock reset signals used multiplier having same output is being replaced by single multiplier unit hence it is more beneficial as hardware requirement is less and circuit complexity is less compared also power required is less compare with the previous

3. Result Analysis

3.1Compilation Report of Filter 1 And Filter 2

Specifications	***Filter 1***	***Filter 2***
Entity Name	*Fpgaimp1*	*Fpgaimp2*
Family	*Cyclone*	*Cyclone*
Device	*EPIC6Q240C7*	*EPIC6Q240C7*
Total logic elements	*508/5980 (8%)*	*492/5980(8%)*
Total Pins	*51/185(28%)*	*20/185(11%)*

3.2 Output Wave Form Of Filter 1 & Filter2



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3.3 Power Optimization Report of Filter 1 and Filter 2

Specification	*Filter 1*	*Filter 2*	*Power Optimized*
Total thermal Power dissipation	*133.81 mW*	*104.44 Mw*	*21.949%*
Core Dynamic thermal Power dissipation	*7.87 mW*	*5.94 mW*	*24.523%*
Core Static thermal Power dissipation	*60.00 mW*	*60.00 mW*	*0*
I/O thermal Power dissipation	*65.94 mW*	*38.49 mW*	*41.628%*

4. Conclusions

In this paper, we introduced the formalization for designing digit-serial FIR filter operation with optimal area at the gate level by considering the implementation costs of digit-serial addition, subtraction, and shift operations. Since there are still instances with which the exact CSE algorithm cannot cope, we also proposed an approximate GB algorithm that finds the best partial products in each iteration which yield the optimal gate-level area in digit-serial MCM design. This paper also introduced the design architectures for the digit-serial MCM operation and a CAD tool for the realization of digit-serial MCM operations and FIR filters.

The experimental results indicate that the complexity of digit-serial MCM designs can be further reduced using the high-level optimization algorithms proposed in this paper. It was shown that the realization of digit-serial FIR filters under the shift-adds architecture yields significant area reduction
when compared to the filter designs whose multiplier blocks are implemented using digit-serial constant multipliers. It is observed that a designer can find the circuit that fits best in an application by changing the digit size. By using this we can easily reduced the power consumption and also the hardware implementation cost and complexity.

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