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ASIC Design Using Programmable Interconnects Based On CBRAM

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***Abstract*— This work evaluates the performance of CBRAM(Conductive Bridging Random Access Memory) based architecture for ASIC (Application Specific Integrated Circuit). In everyday life we completely depend on the VLSI(Very Large Scale Integrated Circuits) chips that drives our electronic devices such as microwaves, mobile phones and ICs that drives our vehicles. So it is necessary that the programs that drive the work should be burned to the chip in a faster way. In general case of the ASIC devices the speed of programming the device is entirely depend upon the interconnect network that are present inside the memory devices for example the EEPROM(Electrically Erasable Programmable Read Only Memory).The interconnect networks consist of SRAM(Static Random Access Memory) network that bridges the switch block and logical block. By the usage of SRAM it will consume more amounts of power and thus forming a boundary to achieve higher speed. This conventional design of ASIC using SRAMs can be overcome with the help of replacing the SRAMs with the CBRAM. By doing such the programming speed will be increased and also the power consumption will be greatly reduced in this design.**

***Index Terms*— Non Volatile Memory, Programmable Interconnects based designs, Application Specific Integrated Circuits(ASIC), Static Random Access Memory(SRAM)**

I. Introduction

Over the past decades in VLSI field the systems are said to be made up of SRAM based designs, for example the conventional design of FPGA consist of SB(Switch Block),CB (Control Block) and LB(Logic Block). These blocks are said to be consisting of SRAM based design, the disadvantage of these type of designs are said to be consuming more amount of power also these designs are said to be more floor area of fabrication. The design that is proposed by the work [1] designed a new FPGA system that is designed using a nonvolatile memory block called as the RRAM (Resistive Random access Memory). The design proves to be a better substitute than the conventional SRAM based FPGA, the area that are required to fabricate are smaller. But the RRAM does have the barrier in the physical design domain. The fabrication process involves in the fabrication of the RRAM at the foot of the selected transistor.

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This may sound easy but in real case it is quite harder. So the work required a special routing algorithm. The nature of the algorithm is said to be more complex to solve the physical design constraints. So to overcome this kind of tedious process CBRAM just eases the design process. It is notable that the CBRAM are proven to be a better performer than the previous works done by [2] -[5].

II. Why Preferring ASIC

The previous work are constructed for the FPGA framework, we know that FPGAs are test equipment. Our idea is to concentrate on real time applications, so that we can able to design an real time system to working at higher speed. A ASIC is so called Application Specific Integrated Circuit, these systems are said to be designed to perform a specific task for example a chip is designed to control the ABS of a bike will perform that task alone. When someone tries to use it for other functions the hardware fails to work out. The idea of the work will increase the programming speed of the device. For instance on considering a critical programming conditions like the time taken for programing a SoC(System on Chip) a DSP processor with highly complex codes will take time for the chip to perform the action, if this delay are carried in a real time situation it will end up it a major loss. So this is the main idea of selecting the ASIC environment.

III. Organization of the Paper

The organization of the paper is carried as follows, CBRAM is discussed in IV, Designing Of SoC(simulations) in V, results VI and conclusion VII.

IV. About CBRAM

The conductive bridging random access memory are said be classified under the group of NVMs(Non Volatile Memory). A NVM have the ability to retain the memory even after the system are powered off, so nowadays these types of memories are required in a higher amount than the volatile type memories. One of the well-known volatile memory is SRAM, we know that this type of memories are requiring higher power to perform the action. That's the main idea for us to change the idea on working with NVMs. Some of the NVMs that are in the research field are CBRAM,SONOS, RRAM, Racetrack memory, NRAM, Millipede memory and FJG.

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A. Selecting the right NVM

There are list of NVMs that are available in the field by the right NVM is required to solve our issue in physical design. We already know that RRAM is not a suitable for this issue. So we are moving to others for suiting up our parameters. Our requirements to select the NVMs are based on the area consumption, power consumption and also the physical design constrains. On analysing the SONOS(Silicon Oxide Nitride Oxide Silicon) the inference is that the device is said to be occupying more amount of area from the work [4].The reason for leaving this out is, the repeated deposition of the blocking oxide(oxygen layer) which are quite tedious in the physical design of the device it will occupy more surface, which makes us difficult to fabricate over the selected transistor. Then another emerging NVM is the Millipede memory from the work [6]-[8].It is seen that this type of NVM are comparatively a higher performer than that of the SONOS. The Millipede memory is consisting of Tb/in which are fabricated over the thin polymer film. The drawback of this design is that it will be highly instable when we fabricate in 3D integration. The reason for us to choose the 3D integration is because in recent trends this design is highly recommended due to its efficient performances.

Moving on to the other NVM the racetrack memory, these designs are build using a smaller blocks and they are called as STT-RAM(Spin Transfer Torque Random Access Memory). These are broadly classified under the NVMs called as MRAM (magnetic Random Access Memory).Analysing from the work [9] it is observed that the design uses the MgO layer which is quite problematic in the physical design constraints. This will be reacting with the SiO layer and it will be causing effect which will be a parasitic issue. On the other hand the design is only 63% energy saving, since we are aiming at a better design we are leaving this NVM. The final left out NVM is the FJG(Floating Junction Gate) from the work [10] this design constitutes a connecting of gated p-n junction diode which is connected to a NMOS/PMOS circuit. The disadvantage of the design is that it is almost similar to the DRAM. We know that the charge dissipation is said to be quite higher in the circuit when compared to SRAM. So this memory is left since it fails to match our selection criteria.

The final NVM that we have to analyse is CBRAM(Conductive Bridging Random Access Memory), it is grouped under the category of PMC (Programmable Metallization Cell). The design is described as coating of inert materials over the SiO layer. Some of the best inert elements are Ag, Chalcogenide, GeS_2 and Si_3N_4. There are also few more of these inert substances we can choose depend on their fabrication possibilities. In this design we are choosing Si_3N_4 and Chalcogenide substances. From the work [11] it is captured that the work is easy to fabricate a 2 Mbit over a 90nm design. The read and write time are quite comprising to us. On looking over the physical design constrains from the work [12] shows us that the CBRAM is quite good performer in 3D space with a easy physical design parameters. The area and the power that are consumed from the work [13]-[16] the power and area parameters are quite adoptable to us.

So from all the reviews on different NVMs we can able to fetch that the CBRAM is quite compromising to our design specifications, so we went ahead and we choose the CBRAM to be integrated over the ASIC platform. The next section will show how to design the work.

V. Designing of SOC (Simulation)

In this work it is totally targeted on the SoC device which was launched by Xilinx in the year 2013 and the target model is Xilinx Zynq 7000 series SoC device. This work enables to adopt the CBRAM to the programming unit of the SoC. The nature of the programing unit in the SoC is constructed with SRAMs and our idea is to replace the SRAMs by the CBRAM, this will produce an outcome of a low power design with lower area consumption.

A. About Xilinx Zynq 7000

Before going in to the description let us review the applications of the SoC in the practical world. It is necessary that modifications that we make the device should perform well and it should be performing at a higher range. The ZYNQ 7000 series got a wider range of applications. Some of the applications of Zynq 7000 are explained in below.

a) Smarter networks: The network modules that we use in our today's life are more complex designs which are said to be performing at a higher end works. This typical SoC are used in Military applications, cockpit and aviation communications. These may consist of GPS for tracking missiles or locating any armed fighter jets coming in way. Since time is the key element in any military operations, for instance the missiles that are coming the way should be locked as soon as possible. If the SoC is not programmed at higher end speed then time lag occurs and eventually this may cause a major problem. The Zynq 7000 do have some advanced wireless applications such as Baseband, small cell , backhaul and some wired communication such as 1588v2 ,OAM,QoS and M2M networking.

b) Smarter Vision: The SoC also got some wide area of applications in the vision based applications. From the vision we can able predict that multimedia is the basic platform for the application of the SoC. Our primary target will be the display equipments such as the monitors. Xilinx have launched DSP based SoC devices on 2013 that as the ability to project or display 4k resolution video or images, but on the market platforms these 4k Televisions hit the stocks on late 2014. When these TVs were feed by high end graphics games or higher frame rate videos, these SoC will lag and it tries to slow down the images. This will make the consumer to be a non satisfactory one. Some other applications such as the DSLR, night imaging and radars in these applications we need high performing systems. For instance the camera should take a picture of fast moving objects such as the missiles or even

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some fast moving objects like planes or jets. If the system is slow then we cannot able to find the object in the frame. Other than multimedia in medical platforms the displays are quite important, for instance in viewing any deformities in scanned image of brain or some other organs.

c) Smarter Control: This is the final application of this session, this involves in SoC being used in Control Modules. The control modules for missiles do stand first in the control modules because at military applications guiding the missiles is first main thing. The possible thing can go wrong will be the guided missiles are tracking the wrong target, this may happen due to the time lag that occurs in the system. Some other applications are Programmable Logic Controller (PLC), motor control and industrial networking. For instance consider the SoC that are widely used in modern electronics control unit (ECU) for bikes and car. The basic function of the ECU will be consisting of ABS, Electronic Throttle Control, Traction Control and GPS. The selected SoC should be performing at higher sensing ability and higher speed because the rider may rev up the machines to top end for higher speed, these SoC should be in synchronous with that speed. If any failure of this synchronizing, it may result in a crash.

B. Designing & Simulations

The tools that are used in designing this work is a T-CAD tool called a Silvaco and a schematic editor known as the Virtuoso provided by Cadence Inc. Silvaco is used to design the and simulate the CBRAM where as the Cadence Virtuoso is used to integrate the CBRAM to the ASIC environment. Fig 1 shows the design flow of this work. The design procedures are explained below.

a) Designing through Silvaco: Silvaco is a typical Technical CAD application that helps us to design a new type of device. It enables the user to define every layer of the extraction that is processed in fabrication. One can change the performance of any basic semiconductor device, some process such as changing the capacitive effect or changing the doping concentration which will eventually affect the device parameters. Understanding the every corner of the semiconductor physics will greatly help in programming phase. The language that are used in this work is said to be called as the "The extraction language". The focused tool that is used here is "Athena" environment this tool helps us to override any manual procedures for design the layers of the device. Another parallel approach will be using the layout design technique but this type of simulations is not quite compromising and not practical. So in this work we have chosen the Athena. Once the coding phase are over then we have to simulate the results. In this tool we do not have that module to simulate so we prefer "Tony Plot", this can easily called to the top module which enables us to simulate the outputs. The main advantage of the tool is that we can enable the device to be integrated to 3D design which is more required for the technologies that are present today. Once we obtain the results we are creating a "Process Design Kit (PDK)" in other words it is called as the ".Lib file" for Cadence schematic or layout editor. First we simulate the normal SRAM based ASIC then we design CBRAM based SoC then we compare it.

b) Designing through Cadence: Once we are ready with the PDK file then we are going to integrate the header file to the Cadence environment. Virtuoso. This tool is analog or mixed typed simulations. First we design the programming block of the Zynq 7000 using conventional SRAMs then we simulate and analyze the parameters. The designing of this phase will be very simple similar to that of the ORCAD PSPICE, it is just placing the components and wire them. Once the whole system is ready then we simulating the design.

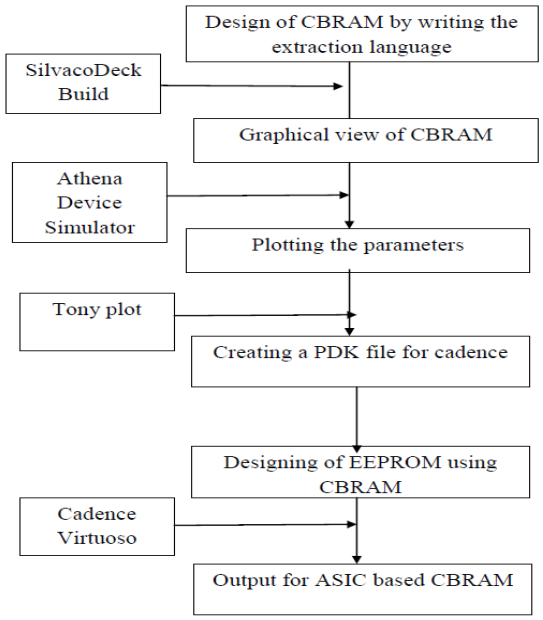

Fig.1 Work flow for designing CBRAM in Silvaco and Cadence

VI. RESULTS

The execution phase involves in the simulation results of the CBRAM, conventional SoC (Zynq 7000) and modified ASIC using CBRAM. In the simulation of the CBRAM various test parameters are taken into account such as the switching parameters and the performance analysis. Fig 2 shows the modeled CBRAM in the Silvaco Athena device modeling platform which shows the intermediate layers that have been modeled, the lower layer forms the substrate and the above layers are said to be the oxides that forms the dielectric medium. Then the above layers are composition of the inert materials. Then design is subjected to different type of analysis which enables us to study the device in depth of the device that we have modeled. Simulations such as the heat radiation of the device will help us to design a low powered device.

In cadence design environment the schematic editor virtuoso we have designed the SRAM based SoC in fig3 and CBRAM based in fig4.The comparative analysis of the CBRAM and the SRAM are shown in the fig7.

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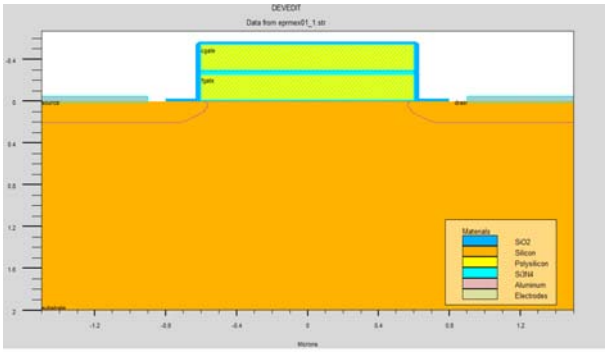

Fig 2 Building up of CBRAM in Silvaco design suite

The above figure shows the layers of Si, SiO_2 and the above layers of the CBRAM are modelled. Here in this work we have designed the inert material layers to be Ag, Chalcogenide, and Si_3N_4 , there are other available materials such as GeS_2. Choosing a typical inert material is explained in the previous sections.

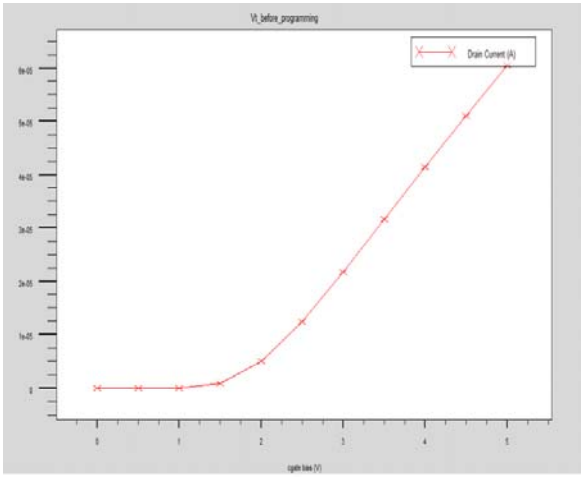

Fig 3 Switching ON of CBRAM

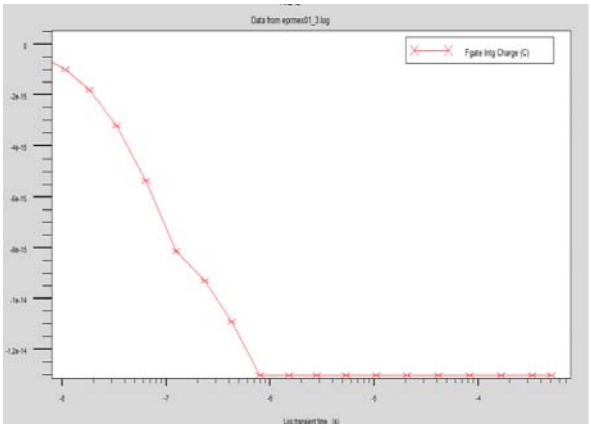

Fig 4 Switching Off of CBRAM

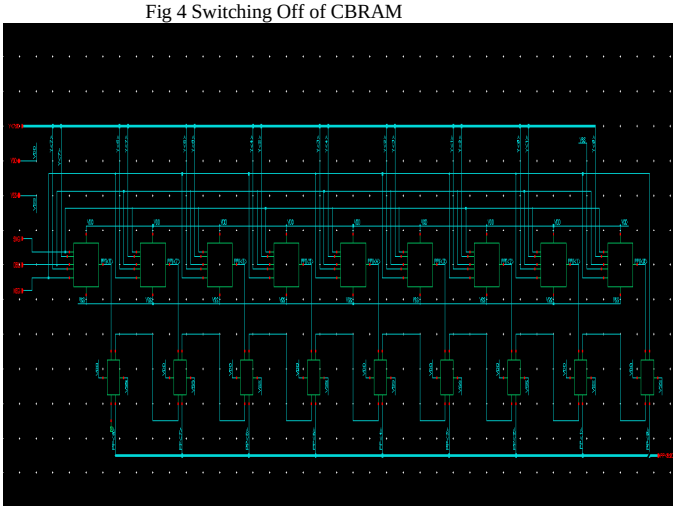

Fig 5 Programming Cell in Zynq 7000 using CBRAM

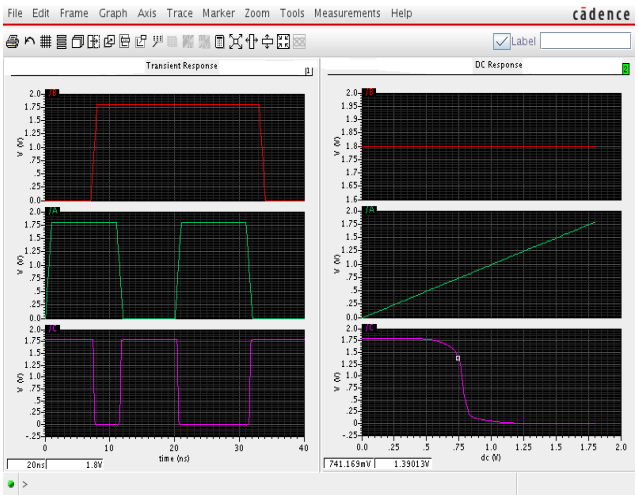

Fig 6 Schematic Analysis and DC response NAND array using CBRAM in programming block of Zynq 700

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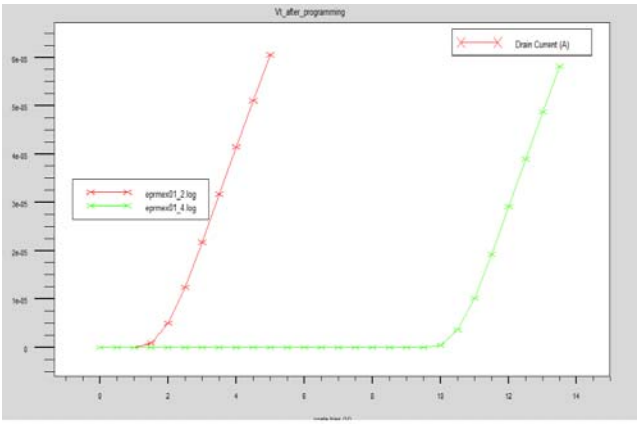

Fig 7 Comparative analysis of CBRAM and SRAM based ASIC

Fig 3 & 4 shows the complete switching analysis of the CBRAM, the output shows that the CBRAM is proven to be a low power device that can perform well even at lower operation voltage. Fig 5 shows the modeling of the NAND array module using the CBRAM in Zynq 7000 programming block. Fig 6 shows the schematic and the DC analysis of the designed programming block. Fig7 shows the final result i.e the comparison of the CBRAM based SoC to the SRAM based SoC device.

VII. Conclusion & Future Work

This work is concluded by the comparison of the CBRAM based SoC to the conventional design i.e SRAM based design and it is proven that the CBRAM is comparatively a better performer than the SRAM. This type of SoC will produce a outcome of high speed programming devices that can be easily adaptable. This work can be further extended by studying the different types of inert compounds that can relatively suit the CBRAM, which may help us to design even higher performing SoC .

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