ISSN 2348 – 7968

A Review on Challenges for MOSFET Scaling

Shivani Chopra[1] and Subha Subramaniam[2]

[1] Department of Electronics Engineering, Shah & Anchor Kutchhi Engineering College, Mumbai, Maharashtra, India

Abstract

This paper provides an overview of the issues faced by the downscaling of MOS devices. For retaining growth in device density, the scaling issues like the power supply and threshold voltage scaling, hot carrier degradation, gate oxide tunneling, random doping fluctuation, high electric field, parasitic resistance and capacitance, source to drain tunneling, short-channel effect should be well understood. A possible way for the microelectronics industry to keep up the high-density pace is to shift from the traditional MOSFET based standards to one based on nanostructures at the molecular level.

Keywords: *Scaling, Nanoelectronics, Short channel effect, Tunneling, Threshold Voltage*

1. Introduction

CMOS technology scaling has been a basic key for continuous progress in silicon-based semiconductor industry. Scaling is followed by Moore's Law since few decades which provided simple rules for transistor design to increase circuit density and speed. The improved circuit performance and density enable more complicated functionality, since more transistors can be integrated on one single chip. However, as device scaling continues for the 21st century, it turns out that the historical growth, doubled circuit density and increased performance followed by Moore's Law cannot be maintained only by the conventional scaling theory. Increasing leakage current does not allow further reduction of threshold voltage, which in turn prevents further supply voltage scaling for the speed improvement. Higher electric fields generated inside of the transistor worsen device reliability and increase leakage currents. Moreover, the required high channel doping causes significant challenges such as mobility degradation and random dopants induced threshold voltage fluctuations [1].

2. Significant problems in downscaling of MOS devices

The development of MOSFET-based CMOS technology is facing challenges in the further development aiming higher device performances mainly low power consumption and high ON-state current. The improved performance is achieved by reducing the MOS transistor's dimensions. MOSFETs dimensions are going down from submicron to nanometer scale. However, the drastic dimension reduction will not always comply with device performances and poses problems that are yet to be solved.

2.1 Power supply and Threshold Voltage

The MOSFET channel down-scaling tends to involve proportional reduction in supply voltage to keep electric field and active power within limits. However, the threshold voltage cannot be scaled down much. This is because the passive power (due to transistor off-state leakage) constitutes a significant portion of the total power dissipation in high performance CMOS products. The major power consumed in this state is due to leakage current through the device. Therefore, V_T scaling has slowed down to avoid dramatic increase in I_{OFF}. To achieve large drive current, the gate overdrive ($V_{DD} – V_T$) needs to be significant and therefore V_{DD} scaling also has to slow down, which results in increase active power density [3].

2.2 High electric fields

As mentioned above, the supply voltage cannot be reduced in proportion to channel length, hence the scaling will increase the electric field strength across the gate oxide. Carrier mobilities are degraded due to higher vertical electric fields in MOSFET channel which in worst cases can cause breakdown of the barrier and hence higher leakage currents which can cause damage to the device.

2.3 Gate oxide tunneling

Since the electron thermal voltage, *kT/q*, is a constant at room temperature, the ratio between operating voltage and the thermal voltage shrinks with scaling down of MOSFET. This leads to higher leakage currents stemming from the thermal diffusion of electrons. With reduction in channel lengths, an appropriate reduction in oxide thickness is also needed. The thin oxide films subject to quantum mechanical tunneling, giving rise to gate leakage current that increases exponentially as the oxide thickness is scaled down. Further scaling can be realized by

replacing the oxide gate dielectric with a high-permittivity (high-k) gate dielectric.

2.4 Parasitic resistances and capacitances

As transistor dimensions are reduced, parasitic resistances and capacitances both scale unfavorably with reduced pitch. Therefore, influence of parasitic elements on on-current increases significantly. These parasitic elements will diminish the performance gain by transistor scaling.

2.5 Hot-carrier

When carriers possess high energies having effective temperature greater than the lattice temperature, they are said to be *hot*. These carriers are not in thermal equilibrium with the lattice because they cannot transfer their energies to the lattice atoms fast enough. They are generated in inverted channel region when MOSFET is operating in linear or saturation mode. The main problems which arise due to hot carriers are parasitic gate currents, drain current degradation, decrease in transconductance, shift of threshold voltage with time. Using graded drain profile reduces generation of hot carriers [4].

2.6 Randomness of dopant distribution

The affect of randomness of dopant distribution on the MOSFET characteristics becomes more extreme in small devices, because precise position of the individual dopant atoms cannot be managed. So, as the device dimensions are reduced it becomes difficult to place the dopant atoms at exact and required positions.

2.7 Source to drain tunneling

If the MOSFETs channel length between source and drain becomes small enough for electrons to tunnel through the barrier without the gate bias, it can no longer be operated as a switch. Device scaling should be carried out with appropriate limits on dimensions for proper behavior [7].

2.8 Heat dissipation

MOSFETs release their energy in the form of heat in the resistive parts. If this heat is not dissipated properly, *hot spots* are created on the circuit which cause the material to overheat resulting in malfunction of device.

2.9 Interconnect delays

Reduction of the wire width increases the resistance and hence increases the delay. This reduces the speed and hence device may not function much faster due to large interconnect delays. The purpose of scaling is not only to increase the device density on chip but also to increase its speed [6].

2.10 Short-channel effect

As the channel length becomes comparable to the source-substrate or drain-substrate depletion depth, the total amount of depletion charge in the substrate decreases. This results in reduction of threshold voltage [4].

3. Conclusions

As the device scaling is approaching its physical size limitations, various researches have been actively carried out to find an alternative way to continue Moore's law. The technology cycle is getting slow down due to increasing power consumption, process variation, and fabrication cost. Nowadays device scaling tradeoffs between performance and power consumption, therefore technological innovations which can achieve high performance through very low power are required. If some efforts are being made to maintain the advanced CMOS technology, it cannot go beyond few decades. Hence emerging devices should be considered in order to comply with technology developments in the near and far future.

References

[1] Yong-Bin Kim, "Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics", Trans. Electr. Electron. Mater. 10(1)21(2009): G.-D. Hong *et al.*

[2] ITRS Roadmap 2010; www.itrs.net.

[3] Xin Sun, "Nanoscale Bulk MOSFET Design and Process Technology for Reduced Variability", Ph.D. thesis, Electrical Engineering and Computer Sciences, University of California, Berkeley, 2010.

[4] V K Khanna, "Emerging trends in ultra-miniaturized CMOS (Complementary metal-oxide-semiconductor) transistors, single-electron and molecular-scale devices: A comparative analysis of high-performance computational nanoelectronics", Journal of Scientific &Industrial Research, Vol. 63, October 2004, pp 795-806.

[5] G. E. Moore, Electronics, Vol. 38, No. 8, April 19, 1965.

[6] Tezaswi Raja, Vishwani D. Agarwal and Michael L.Bushnell, "A Tutorial on the Emerging Nanotechnology Devices", Dept. of ECE, Rutgers University, Piscataway, New Jersey, USA.

[7] Subha Subramaniam, R.N Awale and Sangeeta M. Joshi, "Drain Current Models for Single-Gate MOSFETs & Undoped Symmetric & Assynetric Dopuble-Gate SOI MOSFETs and Quantum Mechanical Effects",

International Journal of Engineering Science & Technology, Vol. 5, No. 1, January 2013.

Shivani Chopra was born in Jammu district, Jammu & Kashmir, India.She received her B.E. degree in Electronics and Telecommunication from Marathwada Mitra Mandal College of Engineering affiliated to University of Pune in May 2013. She is currently pursuing M.E. degree in the Department of Electronics, University of Mumbai, India, duration 2013-2015.

Subha Subramaniam was born in Nagercoil, Kanyakumari district, TamilNadu, India. She received B.E degree in Electronics and Communication Engineering from Govt. College of Engineering (GCE), Tirunelveli affiliated to Anna University in July 1998 and M.E degree in Electronics Engineering from Thadomal Shahani Engineering College (TSEC), Mumbai affiliated to Mumbai University in Nov 2003. She is currently pursuing Ph.D in Electronics Engineering from Veeramata Jijabai Technological Institute (VJTI), Mumbai. Presently she is working as Associate professor, Department of Electronics at Shah & Anchor Kutchhi Engineering College (SAKEC), Mumbai. Her research interest is in the area of Nanoelctronics.