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An Asynchronous High Performance FPGA Based on LEDR/Four Phase Dual Rail Hybrid Architecture

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***Abstract* – In today's fast growing world, efficiency and speed plays a major role. Asynchronous design has been used to overcome various problems occurred due to synchronous architectures. An asynchronous high-performance Field Programmable Gate Arrays(FPGA) that combines Four-Phase Dual-Rail (FPDR) protocol and Level-Encoded Dual-Rail (LEDR) protocol. FPDR protocol is employed to get a small area for logic blocks and LEDR protocol is employed to obtain high bit rate and low power for data transfer. Each logic block consists of LEDR to FPDR protocol converter, FPDR to LEDR protocol converter and two pipelined FPDR LUTs that operates alternately. The proposed FPGA is designed using Xilinx and the simulation result shows that the output is 3.91 GHz.**

Keywords
Asynchronous circuit, domino logic, Four-Phase Dual-Rail (FPDR) protocol, Level-Encoded Dual-Rail (LEDR) protocol, reconfigurable VLSI

I. INTRODUCTION

Most digital circuits designed and fabricated today are 'synchronous', which means, they are based on two fundamental assumptions that greatly simplify their design: (1) all signals are binary, and (2) all components share a common and discrete time, as defined by a clock signal distributed throughout the circuit.

Asynchronous circuits are fundamentally different ,they also assume binary signals, but there is not common and discrete time. Instead of that the circuits use handshaking between their components in order to perform the necessary synchronizing, communicating, and sequencing of operations. Expressed in synchronous terms it results in a behavior that is similar to systematic fine-grain clock gating and local clocks that are not in phase and whose period is determined by actual circuit delays registers are only clocked where and when needed.

Field-programmable gate arrays (FPGAs) are widely used to implement special-purpose processors. FPGAs are cost-effective for small to lot production because functions and interconnections of logic resources can be directly programmed by end users. Even its design cost advantage, FPGAs exhibit slower operating speed compared to custom silicon alternatives because of programmable interconnects fine-grained pipelining is an effective approach to improve throughput but it requires a more number of registers. Hence, it is difficult to apply fine-grained pipelining to conventional synchronous FPGAs which have large numbers of registers and complex clock distribution networks. To solve the problem, asynchronous FPGAs have been proposed. Instead of using the clock the asynchronous FPGAs use the handshake protocol between their components to perform the necessary synchronizing, communicating, and sequencing of operations. Most of the high-throughput asynchronous FPGAs use Four-Phase Dual-Rail (FPDR) protocol the reason is it has simple hardware of the function units. However, in FPDR protocol, a spacer must be inserted between two consecutive data values. It results in low throughput and large power

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consumption of the data transfer using the programmable interconnection resources because of the large number of signal transitions. Another well-known dual-rail protocol is Level-Encoded Dual-Rail (LEDR) protocol which does not require spacer. As there is no spacer, the number of signal transitions is half that of FPDR protocol, which results in the throughput and the power consumption of the data transfer using the programmable interconnection resources are small. But, the drawback of LEDR protocol is its complex hardware of function units. In this paper, we proposed a high-throughput asynchronous FPGA that combines FPDR protocol and LEDR protocol, here the basic idea is focused on improving energy consumption. This architecture is focused on high performance and efficient data transfer. Level Encoded Dual Rail protocol is used to obtain high throughput and efficient data transfer between LBs, while FPDR protocol is used to achieve small Logic Blocks (LBs). In addition, fine-grain pipelined LB, dual pipeline technique and interconnects are introduced to improve the performance. According to the simulation result the proposed FPGA will operate upto 3.91GHz.

II. METHODOLOGY

The overall structure of the proposed FPGA is shown in figure 1.The FPGA comprises of regularly arrayed cells. Each cell is connected to adjacent eight cells through input and output channels. However, LEDR protocol is employed for data transfer, a channel requires three wires to transfer a single data bit.

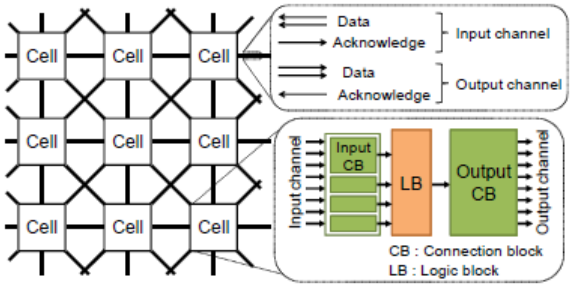

Figure 1: Overall structure

A cell consists of four Input Connection Blocks (CBs), an Output CB and an LB. Figure 2 shows structures of Input CB and Output CB. The Input CB comprises of MUXs and takes LB's input from input channels connected to adjacent eight cells. The Output Connection Block consists of DEMUXs and distributes LB's output to output channels. Since MUXs and DEMUXs work as LEDR registers, Input CB and Output CB behave as 2 and 3-stage pipeline. A Logic Block (LB) structure is proposed in figure 3.The proposed Logic Block consists of LEDR to FPDR converter, two 4-input FPDR LUTs and FPDR to LEDR converter. As mentioned earlier, FPDR protocol is employed to achieve small area for LUTs, while LEDR protocol is employed to achieve high throughput and low power for data transfer. In the LUT, the spacer of FPDR protocol is required. Hence, in a typical manner, the throughput of the hybrid architecture is almost same as the FPDR based architecture despite it employs LEDR protocol for the fast data transfer.

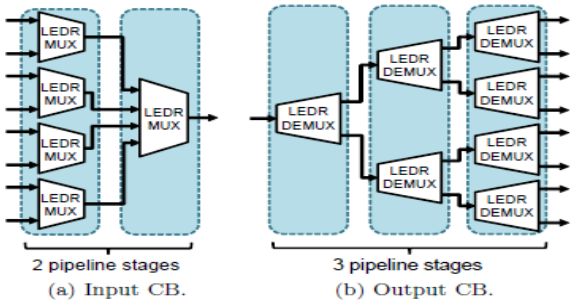

Figure 2: Structures of CBs.

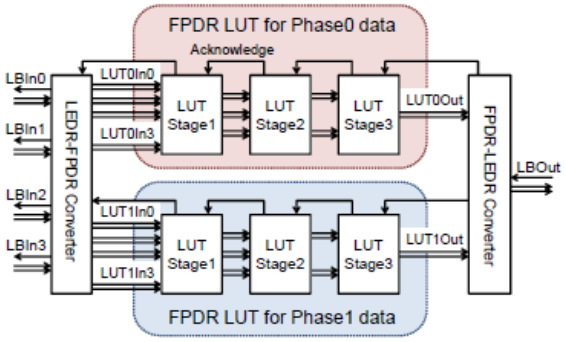

Figure 3: Structure of a proposed LB.

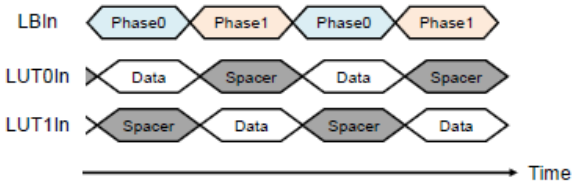

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Figure 4: Time chart of an LEDR-FPDR converter and LUTs.

To solve this problem, dual pipelined architecture is employed. As shown in Figure 3, the FPDR LUT is duplicated and they execute boolean operation alternately. Figure 4 shows the time chart of an LEDR-FPDR converter and LUTs. When the phase of the LBIn is 0, the LEDR-FPDR converter sends valid data to LUT0 and it sends a spacer to LUT1. When the phase of the LBIn is 1 the LEDR-FPDR converter sends valid data to LUT1 and it sends a spacer to LUT0. In a similar manner, output data from LUTs are converted by FPDR-LEDR converter continuously. Hence, the delay caused by the spacer is concealed, a high performance FPGA based on a dual pipeline architecture employs FPDR protocol and requires five wires (four wires for data and one wire for an acknowledge signal) to transfer a single bit data. Hence, the proposed architecture is more efficient at data transfer between LBs.

III.SIMULATION RESULT

Each LB mainly consists of a LUT, an output register, a sleep controller, and a C-element. The LUT operates arbitrary two-input and one output logic functions. The C-element is a state-holding element for handshake protocol. The gray region is the sleep controller. The *Wake-up* signals from previous LBs are used to wake up the LB before the new input data arrives. The *Data-arrive* signal is used to wake up the next LB when the data arrives. In the sleep mode, all pass-transistors turn off according to the outputs of the decoders; the outputs of multiplexers are in the high impedance condition; the latches keep the previous operation result, shown in fig 5(a) & 5(b).

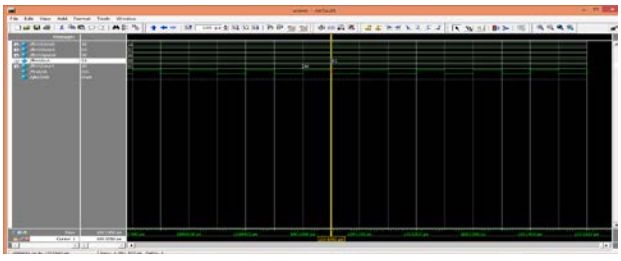

Figure 5(a)

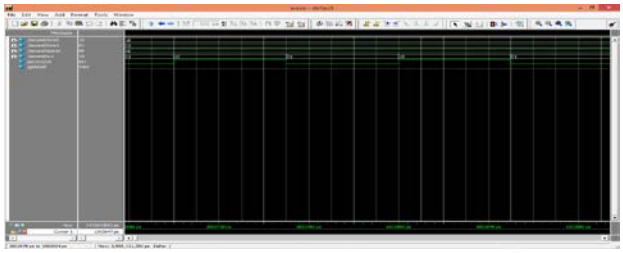

Figure 5(b)

Figure 5(a) & 5(b):Simulation of FPDR/LEDR hybrid Protocol

IV. CONCLUSION

This paper proposed an asynchronous high-performance FPGA that combines FPDR protocol and LEDR protocol. LEDR protocol is employed to achieve high throughput and efficient data transfer between Logic Blocks (LBs), while FPDR protocol is employed to achieve small LBs. Moreover, fine-grain pipelined LB, interconnect and dual pipeline technique are introduced to improve throughput. The simulation result shows that the maximum throughput of the proposed FPGA is 3.91 GHz. As a future work, we are evaluating the proposed architecture on some practical bench marks. Developing the CAD environment for asynchronous FPGAs is also important topic.

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