IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 2 Issue 6, June 2015.
www.ijiset.com
ISSN 2348 – 7968

A New Enhanced delayed lock loop Design using stand by switch for reduced sub-threshold leakage current

[1]B.Manthru Naik [2]Shaik.Jagadeesh Babu
[1]. Final M.Tech student,ECE,IITS,Markapur,A.P,India.
[2]. Asst.Professor,ECE,IITS,Markapur,A.P,India

Abstract— Dual threshold voltages domino design methodology utilizes low threshold voltages for all transistors that can switch during the evaluate mode and utilizes high threshold voltages for all transistors that can switch during the pre charge modes. We employed standby switch can strongly turn off all of the high threshold voltage transistors which enhances the effectiveness of a dual threshold voltage CMOS technology to reduce the sub threshold leakage current. An ultra wide-range delay-locked loop (DLL) has been fabricated in 70nm CMOS technology. The modified standby reduction delay unit(SRDU) can easily generate a large propagation delay to reduce the difficulties to build up the high-speed digital counter in the cycle-controlled delay unit (CCDU) for a very low-frequency operation. The proposed DLL circuit can operate from 500 KHz to 1 GHz, and the power consumption is verified using Micro wind & DSCH simulation results under the process of 70nm technology thus the efficiency of the circuit is verified and compared with the DLL made up of 65nm technology.

Keywords: All digital delay-locked loop (ADDLL), digital controlled delay line, cycle-controlled delay unit, wide-range operation.

I.INTRODUCTION

The main objective of this thesis is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as

ISSN 2348 – 7968

important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit. Device miniaturization and the rapidly growing demand for mobile or power-aware systems have resulted in an urgent need to reduce power supply voltage (Vdd). However, voltage reduction along with device scaling is associated with decreasing signal charge. Furthermore, increasing intra-die process parameter variations, particularly random dopant threshold voltage variations can lead to large number of fails in extremely small channel area memory designs. Due to their small size and large numbers on chip, SRAM cells are adversely affected. This trend is expected to grow significantly as designs are scaled further with each technology generation. Delay-Locked Loops (DLLs) and Phase-Locked Loops (PLLs) are widely used in high-speed microprocessors and memory interfaces to eliminate the clock skew. To meet the specifications in different applications, the DLLs are desired to achieve wide frequency range especially in low-power system-on-a-chip (SOC) with dynamic voltage and frequency scaling (DVFS). Traditionally, DLLs are often designed with the charge pump-based architecture [1]. However, the charge pump-based DLLs suffer from serious leakage current problem in 65nm CMOS process and the jitter performance becomes unacceptable. As a result, the low leakage CMOS process is often needed when implementing the charge pump-based DLLs in 65nm CMOS process. But if the low leakage CMOS process is used, the circuit performance will be degraded, too. Hence, the all-digital DLLs which use robust digital control code to control the digital controlled delay line (DCDL) can avoid the leakage current problem and become more and more popular now.

Recently, however, as the supply voltage approaches 1 V, conventional scaling has deviated from ideal constant-field scaling due to the difficulty of further lowering the thresh-old voltage (V_{th}). This fundamental problem stems from the non scalable characteristic of the thermal voltage ($V_T = kT/q$), which causes relatively fixed sub threshold swing (S) at the constant temperature [2,4]. This, in turn, makes the sub threshold leakage current exponentially increase as the V_{th} reduces. Therefore, there exists a lowest possible value of V_{th}, which is determined by the application constraints related to power consumption and circuit functionality. In addition, with the knowledge of increased V_{th} variation in nano scale MOSFETs, it is necessary to keep enough margins for V_{th} variation to ensure that V_{th} stays well away from the lowest possible value of V_{th} [3]. In particular, for high-performance (HP)

ISSN 2348 – 7968

logic technology, it is required to keep a certain level of the overdrive voltage ($V_{DD} - V_{th}$), which determines the drive current and hence the performance in a chip. This makes it difficult to accomplish the further scaling down of the supply voltage. Under fixed V_{th}, the reduction of V_{DD} trades off performance (speed) and leakage power.

This trend in technology scaling has made us enter a new era in achieving HP under constrained power 4. Among the leakage power reduction techniques, the reverse body biasing (RBB) technique, which increases the thresh-old voltage (V_{th}) of transistors during standby mode, has widely been employed to suppress the sub threshold leakage current (I_{SUB}). However, this technique also aggravates short channel effects (SCEs), such as drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL), and band-to-band tunneling (BTBT) current. In particular, GIDL and BTBT current significantly increase under the reverse body bias condition since the state-of-the-art MOSFETs are fabricated with high overall doping concentration, lowered source/drain junction depths, halo doping, high-mobility channel materials, etc. Furthermore, the reduction of the gate oxide thickness (t_{ox}) causes a drastic increase in the gate tunneling leakage current due to carriers tunneling through the gate oxide, which is a strong exponential function of the voltage magnitude across the gate oxide. Consequently, to minimize the leakage power in standby mode, those leakage components have to be taken into account when the RBB technique is used.

The adaptive RBB technique has been proposed. However, the previous techniques require significant circuit modification and performance overhead for leakage reduction, and they have not been complete or robust enough to apply to very large scale integration (VLSI) systems since all the leakage-current components and minimum supply voltage are not considered for leakage power reduction. While 16 shows that the leakage power can significantly be decreased using both optimum power supply voltage and optimal body bias voltage, it requires a lot of circuit overhead. Therefore, this paper proposes a new standby leakage power reduction technique applicable to VLSI systems by exploiting the body bias voltage scaling only while all the other leakage currents are taken into account. The proposed approach significantly reduces the required hardware compared with by optimizing the body

ISSN 2348 – 7968

bias voltage only at the cost of efficiency of the standby current minimization the structure of the proposed LDU is shown below.

II. OVERALL CIRCUIT DESCRIPTION

The block diagram of the existing ultra wide-range all digital delay locked loop (ADDLL) is shown in Fig. 1. It is composed of the phase detector (PD), the controller and the digital-controlled delay line (DCDL). The digital controlled delay line is composed of four delay units: leakage delay unit(LDU), cycle-controlled delay unit (CCDU), coarse delay unit(CDU) and fine-delay unit (FDU).

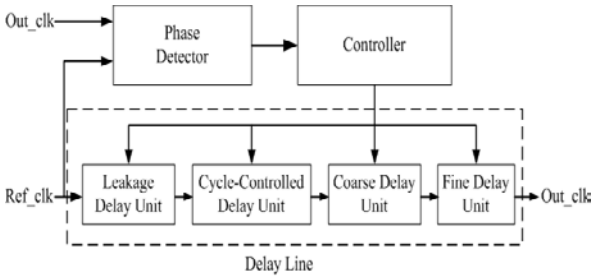

Fig 1: Block Diagram of Existing DLL

The reference clock (Ref_clk) is passed through the delay line and then outputted as Out_clk. The phase detector detects the phase relation between the reference clock and the output clock, and then it outputs up and down control signals to the DLL controller. The DLL controller changes the control code of the DCDL according to the PD's output to eliminate the phase error between the reference clock and the output clock. And when the phase error between the reference clock and the output clock is eliminated, the DLL is locked. When the DLL is used in clock de skew applications, the clock-tree buffer delay is added after the output clock and before the phase detector so that the clock skew can be cancelled. In the existing DLL architecture, the proposed leakage delay unit (LDU) is used to provide a large delay in the DCDL, and therefore the operating range of the DLL can be extended to a very low frequency. And in the conventional shift-register controlled DLL, the sequential search are often used to find the proper control code and resulting in a long lock-in time. The sequential search scheme is not suitable for wide-range DLL, and therefore the binary search scheme is used in the DLL controller to shorten the lock-in time of the DLL.

ISSN 2348 – 7968

III. CIRCUIT IMPLEMENTATION

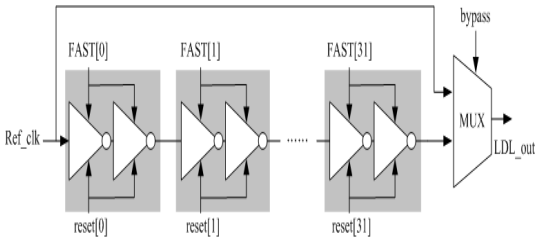

Fig .2.1:Leakage Delay Unit (LDU)

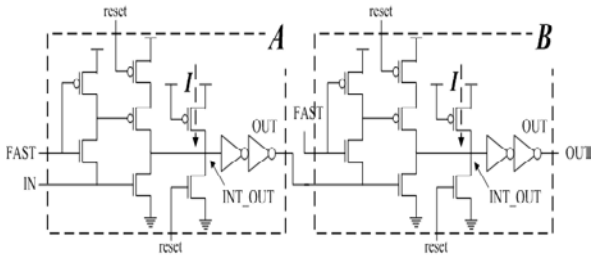

Fig. 2.2: Schematic of the existing leakage delay cell

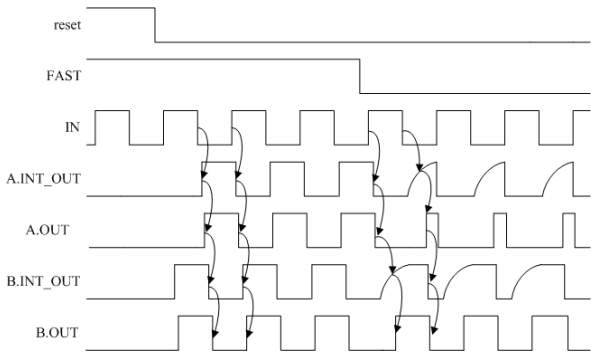

Fig .2.3: Timing diagram of the existing leakage delay cell.

The charging speed can be tuned by adjusting the width of the always-off PMOS transistor. The charging speed is also influenced by process, voltage, and temperature (PVT) variations. In the proposed leakage delay unit (LDU), the maximum delay is generated when FAST is

ISSN 2348 – 7968

32’h0 and the minimum delay is generated when FAST[31:0] is 32’hFFFF_FFFF.

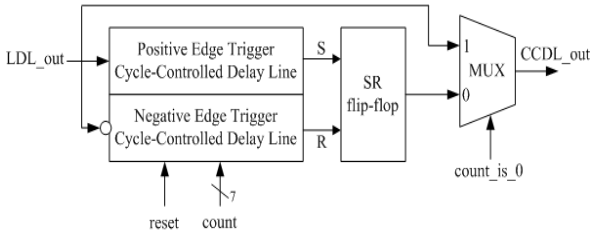

Fig. 3.1: shows the architecture of the proposed cycle-controlled delay unit (CCDU)

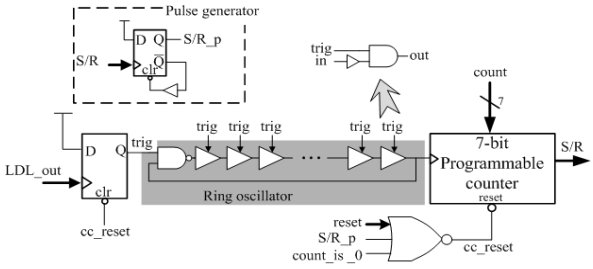

Fig.3.2: shows the detail circuit of the positive edge triggers cycle-controlled delay line.

The proposed CCDU is composed of the positive edge trigger cycle-controlled delay line and negative edge trigger cycle-controlled delay line, SR latch and 2-to-1 multiplexer .The input signal LDL out triggers these two edge-triggered cycle-controlled delay lines at positive and negative edge respectively. As the trigger signal comes, the inner counter will start counting upward until it counts up to the input count value from the DLL controller. While the inner counter matches the count value, the signal "S" and the signal "R" are generated by these two edge-triggered cycle-controlled delay lines. These two signals with a SR-latch can generate an output clock with 50% duty cycle as shown in Fig. 4(c).

ISSN 2348 – 7968

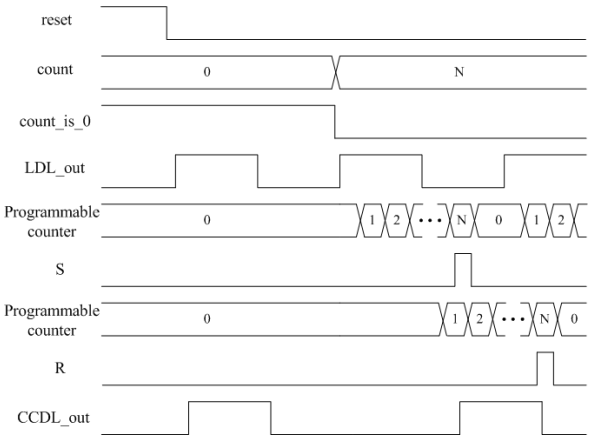

Fig.4: SR-latch can generate an output clock with 50% duty cycle

When DLL is in high frequency operation, the DLL controller will sent zero counter value to the CCDU, and then the signal "count_is_0" is pulled high, and the input signal "LDL_out" is bypassed to the output of the CCDU. In the proposed CCDU, the ring oscillator with the digital counter can generate a large delay for covering the one delay step of previous leakage delay unit in PVT variations.

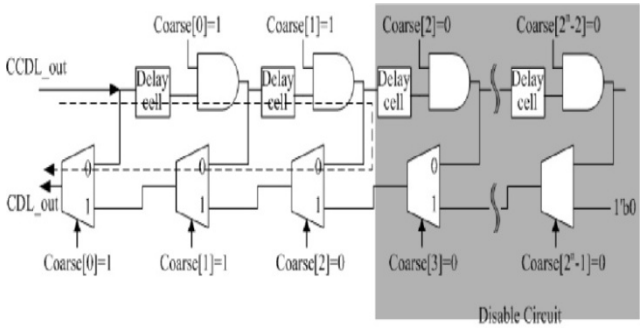

Fig. 5 : The coarse delay unit (CDU).

Fig. 5 shows the circuit of the coarse delay unit (CDU). It is composed of 31 delay cells, 31 AND logic gates and 32 multiplexers. The proposed circuit can generate 32 different delays, and the minimum delay is one multiplexer propagation delay. Unused delay cells can be turned off for reducing power consumption. The total delay controllable range of the CDU should cover the delay step of the previous cycle-controlled delay unit in PVT variations.

Fig. 6 shows the fine delay unit (FDU). It is composed of N cascading buffers and (N-1) digital-controlled varactor (DCV) cells. For better resolution and linearity of the delay line,

ISSN 2348 – 7968

DCV cells are used in fine tuning stage. The total delay controllable range of the FDU should cover the delay step of the previous coarse delay unit in PVT variations.

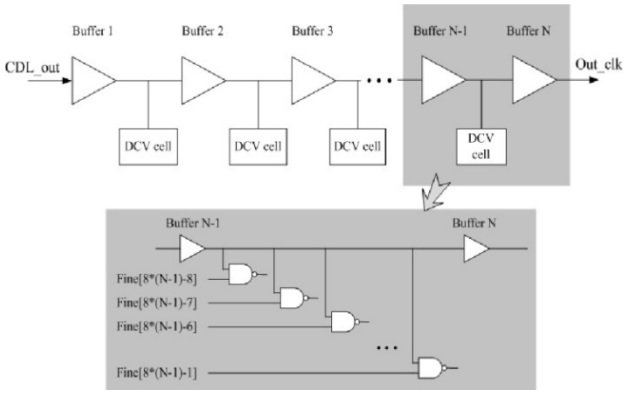

Fig. 6: shows the fine delay unit (FDU)

In DLL the leakage delay unit is replaced with stand by leakage delay unit in order to reduce the leakage current problem. In the proposed scheme, a current comparator is used to determine the optimal body bias voltage target assuming the power supply is regulated outside the chip. The body bias voltages for n-MOSFET and p-MOSFET are automatically set by the control system to ensure that the chip dissipates minimal power in standby mode. The proposed scheme uses the current- mode circuit technique to process the active signals in the current domain, and it offers a number of advantages, such as better sensitivity, high speed, and low-power dissipation Since the circuits used in the proposed scheme are fully analog circuits, and the feedback loop continuously works, no control circuits are required. This is one of the main advantages of the proposed approach

The leakage monitoring circuit separates the sub threshold leakage (I_{SUB}) and the BTBT leakage current ($I_{BTBT1,2}$) from the total leakage components

IV.PROPOSED DESIGN&RESULTS USINGMICRO WIND&DSCH

Our idea is to combine these two different technologies & to design a new circuit with much efficiency than the existing two designs. Thus we are designing a new circuit & showing the simulation results of the different technologies as shown below.

ISSN 2348 – 7968

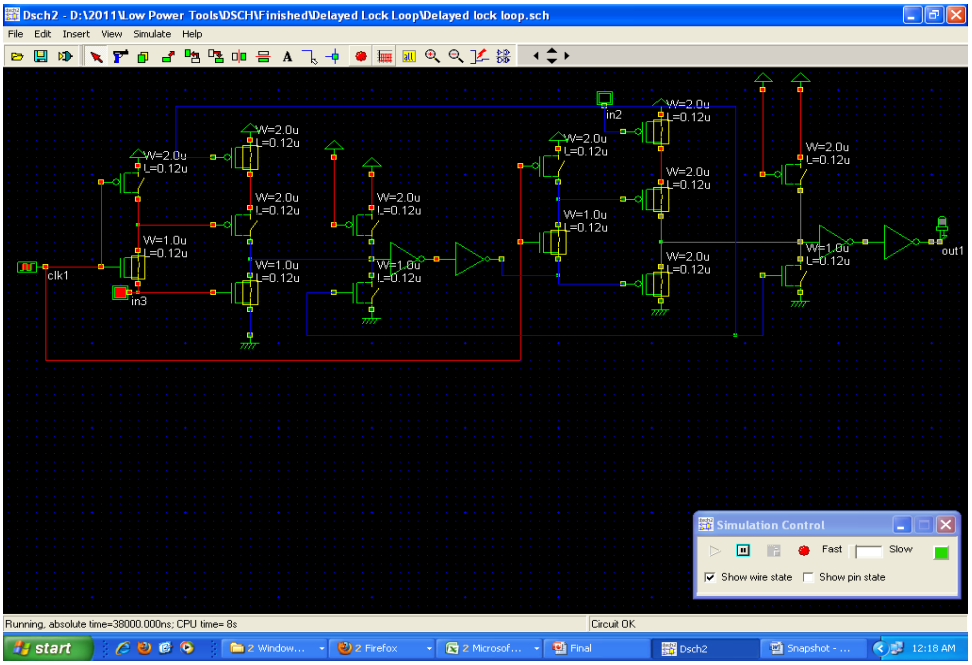

Fig.7: Existing Circuit LDU

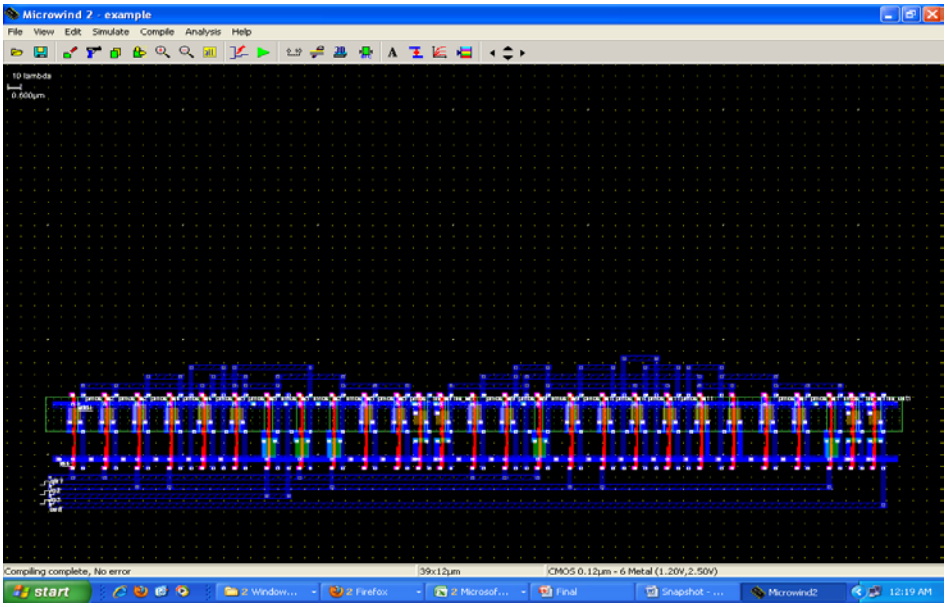

Fig.8: Layout of Existing LDU

ISSN 2348 – 7968

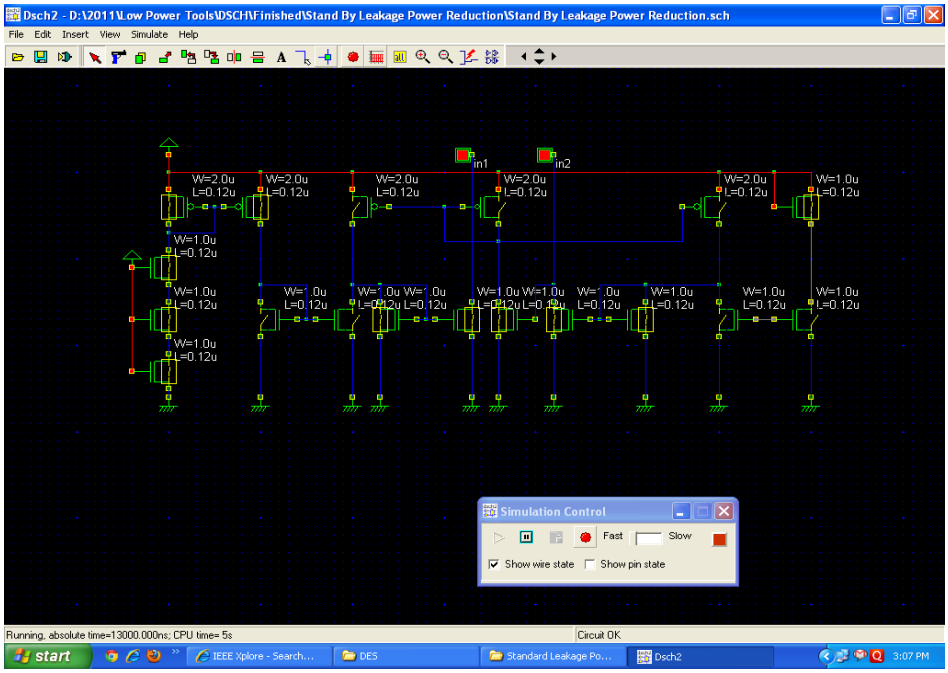

Fig.9: Circuit Implementation of SLDU

V. CONCLUSION

Our proposed design shows that much less power than the existing ones. As the technology scaling goes down below 90 nm, the standby leakage power dissipation has become a critical issue. Therefore, the new circuit design technique for minimizing the leakage power must be developed along with the device scaling. To reduce the standby leakage power, this paper has presented a novel design technique that generates the optimal V_{Body} scaling during standby mode. By monitoring the BTBT leakage current (I_{BTBT}) and the sub threshold leakage current (I_{SUB}), the optimal body-bias voltage is automatically generated and continuously adjusted by the control loop. By tuning the body bias voltage using the leakage-monitoring circuit, the circuit can be biased at the optimal point where the sub threshold leakage current and the BTBT leakage current are balanced to accomplish the

minimum leakage power. The results show that the proposed control system is a viable solution for high-energy reduction in nano scale CMOS circuits. In this paper, a novel **SLDU** cell implemented with 70nm CMOS technology is presented. The proposed Standby leakage Delay unit cell with cycle-controlled delay unit can easily achieve ultra wide frequency range operation. It also achieves smaller chip area and lower power dissipations than previous wide-range DLLs. As a result, it is very suitable for wide-range clock de skew applications in SOC era.

VI. REFFERENCES

[1]. D. A. Antoniadis, I. Aberg, C. N. Chléirigh, O. M. Nayfeh, A.Khakifirooz, and J. L. Hoyt, "Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations," *IBM J. Res. Develop.*, vol. 50, no. 4, pp. 363–376, Jul. 2006.

[2] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H.-S. Wong, "Device scaling limits of Si MOSFETs and their application dependen-cies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.

[3] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEDM Tech. Dig.*, Dec. 5, 2005, pp. 7–15.

[4] W. R. Tonti, "MOS technology drivers," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 2, pp. 406–415, Jun. 2008.

[5] C. Neau and K. Roy, "Optimal body bias selection for leakage improve-ment and process compensation over different technology generations," in *Proc. ISLEP*, Aug. 2003, pp. 116–121.

[6] J. Tschanz, J. Kao, S. Narendra, R. Nair, D. Antoniadis, A. Chandrakasan, and V. De, "Adaptive body for reducing impacts of die-to-die and within-die parameter variations on microprocessor frequency and leak-age," in

[7] M. Nomura, Y. Ikenaga, K. Takeda, Y. Nakazawa, Y. Aimoto, and Hagihara, "Delay

ISSN 2348 – 7968

and power monitoring schemes for minimizing power consumption by means of supply and threshold voltage control in active and standby modes," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 805– 814, Apr. 2006.

[8] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leak-age current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[9] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed.New York: McGraw-Hill, 2001.

[10] S. A. Parke, J. E. Moon, H. C. Wann, P. K. Ko, and C. Hu, "Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model," *IEEE Trans. Electron Devices*, vol. 39, no. 7, pp. 1694–1703, Jul. 1992.

[11] X. Yuan, J. E. Park, J. Wang, E. Zhao, D. C. Ahlgren, T. Hook, J. Yuan, V. Chan, H. Shang, C.-H. Liang, R. Lindsay, S. Park, and H. Choo, "Gate-induced-drain-leakage current in 45-nm CMOS technology," in *Proc. IRW*, 2007, pp. 70–73.

[12] P. J. Wright and K. C. Saraswat, "Thickness limitations of SiO_2 gate dielectrics for MOS ULSI," *IEEE Trans. Electron Devices*, vol. 37, no. 8, pp. 1884–1892, Aug. 1990.