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Error Detection of Eg-Ldpc Codes In Majority Logic Decoding

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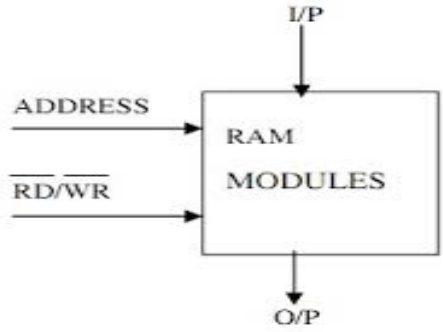
ABSTRACT

Capability to correct large number of errors Majority logic decodable codes is suitable for memory applications. The memory access time as well as area of utilization and the decoding time is reducing using Majority Logic Decoder. In Euclidean Geometry Low-Density Parity-Check (EG-LDPC) codes there exits fault secure detector which are used for error correction. Because EG-LDPC codes are widely used it will avoid high complexity in decoding. majority logic decidable which is a one step is a technique similar to a class of Euclidean geometry low density parity check (EG-LDPC) codes. This method is very effective for EG-LDPC codes as shown in the result. The proposed design of error detection and correction the VHDL is used for coding process and it can be verified as well as synthesize on Modelsim also on Xilinx respectively.

The number of errors are detected by the majority logic decode further it can be used for correct the errors which occurred. This is an Fault secure detector which can be used to detect error and these errors can be corrected by serial one step majority logic decoder. By using sorting network MLDD have the capability of reduces the area of majority gate.

INTRODUCTION

A lots of data has being transferred by using data communications techniques. In communication channels there can be a channel noise, and from these errors may be occurs while transmitting the data from source to destination or we can say from transmitter to receiver. Now-a-days there exits several method which hacks the data during communication. To protect the data confidentiality and to get the data correctly while transmitting data from one source to another if noise occurs the logical values of bit get changed which causes errors in the given device , to avid this condition secure communication is used. There are various types of codes which can detect errors as well as correct it. There are correction codes which are used for multi error bit correction some of them are BCH codes, Reed Solomon codes but in this case the algorithm required by this code is very difficult to compute. For high error detection also for low decoding complexity LDPC codes are used. There is a special type of code which exits in LDPC code is name as Euclidean Geometry-LDPC codes which having the properties of high reliability as well as low area overhead. As the technology increases number of error is also increasing to protect the device from the occurring soft error this code is used. But complex decoder is required to correct this types of error which is directly affecting to system memory. For memory based application one step majority logic decidable codes are used. One step majority logic decoding is serially implemented using simple circuitry but it takes so much of decoding time, ultimately increase the memory access time.



LITERATURE SURVEY

In error detection and correction, majority logic decoding is a used to decode codes it repeats, as it depend on the assumption that the largest number of

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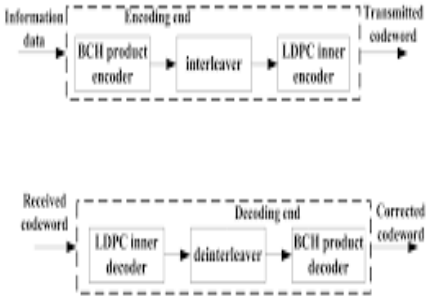
occurrences of a symbol was the transmitted symbol. MLD is based on a number of parity check equations which are orthogonal to each there just because this reason, at every iteration, each and every bit in the codeword only participates in one parity check equation. From the above reason, the result of majority these parity check equations decide the correctness of the current bit under decoding. One parity to check the given equation, avoid the very first bit which constitutes to each and every equations. Because of this particular reason, the result of majority logic decoding of these parity check equations decide the correctness of the current bit under decoding

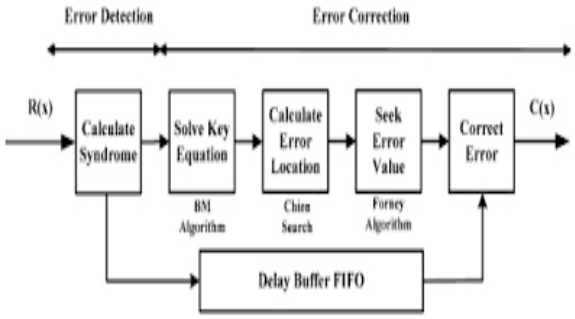


EXISTING SYSTEM

In the existing system correction gate the logical bit to the check equation to detect whether there is an error occurred in the system. After that the check equation which comprise of XOR gate will check the logical bit of the system given from the correction gate, if there is difference between the logical values of gate then it will show error in result. The check equation computed result is given to the majority circuit which detect whether there is error occurred in the system or not, if it occurred in the system then it will display the error to the user. For error detection simple parity check mechanism is used. A parity bit is an redundant bit which is attached to every unit of data. In this process numbers of 1's is added to the data if it contains odd number of parity. In the receiver section firstly the parity bit is computed this received bit is compared. Therefore number of one's is now even, because of this it is called as parity checking

PROPOSED SYSTEM

The proposed design of error detection and correction the VHDL is used for coding process and it can be verified as well as synthesize on Modelsim also on Xilinx respectively.
Over a billion of combinations of errors are tested. As in the existing system we have seen that the system takes full cycle to detect errors. Suppose we consider N=15 then the system will take approximately 15 cycle to reach the final destination, these 15 cycles constitute a single iteration or we can say that one iteration complete. Now as given N=15 it will take 15 cycle to detect the error occurring in the system. So in the existing system unnecessary time is wasting to complete full iteration as same as the number of cycle given. So in our proposed system it will complete approximately four to five iteration and on depending on the probability of the result it will give the error if it is occurred. If there is no errors or the system is error free then its go on checking the logical value of the system and the result shown as error free system



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PROPOSED SOFTWARE

Xilinx ISE (Integrated Synthesis Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize or to compile the designs, process on analysis of time, diagrams examination of RTL,stimuli of different types is used to simulate different design reaction, and the target device configure with the programmer .The Xilinx ISE is a design environment is tightly-coupled for FPGA products from Xilinx, such chips which involves architecture, and cannot be used with FPGA products from other vendors. The Xilinx ISE is primarily used for circuit design and synthesis, for In system-level testing Models logic simulator is used.
Simulation performed in following manner:

System-level testing may be performed with the logic simulator, and the test programs can be written in HDL languages test bench programs may include simulated input signal waveforms, or monitors which take an observation and test the outputs of the device under test.Modelsim may be used to perform the following types of simulation.

- Logical verification, to ensure the module produces expected results
- Behavioral verification, to verify logical and timing issues
- Post-place & route simulation, to verify behavior after placement of the module within the reconfigurable logic of the FPGA.

APPLICATION

It will use in communication system for detection of error and reducing the time required to detect the error. If the decoding length is large then it will take more time to process. By using these code we can detect error fast.

CONCLUSION AND FUTURE SCOPE

In this paper, the detection of errors during first iterations of serial one step Majority Logic Decoding of EG-LDPC codes is presented. The results simulation observe that the one step MLD would takes 15cycles to decode a codeword of 15-bits, which would be excessive for most applications. The MLD design requires small area but requires large decoding time and can able to detect two or few errors. Hence, memory access time increases. Another method, Called MLDD can detect up to five bit-flips and consumes the area of majority gate. The proposed enhanced MLDD have the capability of detecting more than five bit flips and also reduces the area of majority gate by the use of sorting network. At last, the cycle decoding slightly will increase compared to MLDD approach. These two designs are under progress. In Future work we can extend this method to the theoretical analysis for the cases of three and four errors. As it is using for the communication system for detecting the errors as well as to reduce the time required for detecting the error occurred in the memories which ultimately increases the bits required to decode or process. A solution for this facing problem is use of fine-grained between error detection error detection capabilities a decoding time. In this method we are focusing mainly on detection part, in further we can extend it to correction as well.

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