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Design of Low Power CMOS Adder, Serf, Modified Serf Adder

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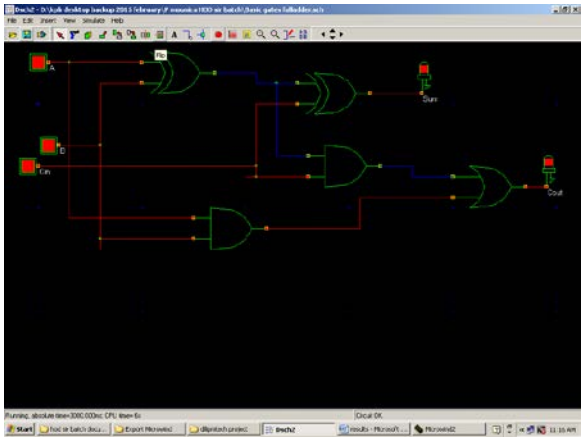
Abstract
In microprocessor and DSP`s, addition is the most commonly used arithmetic operation and it is often one of the speed-limiting elements. Hence optimization of the adder both in terms of speed and/or power consumption should be pursued. In general, CMOS style is the best in terms of robustness and stability. The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this work SERF and modified SERF full adder topology is presented. Basic Full adder, CMOS full adder, SERF adder, Modified SERF adder, Compressor 4:2, 5:2,7:2 are designed..

Keywords:*Adder, CMOS adder, SERF, MODIFIED SERF, COMPRESSOR.*

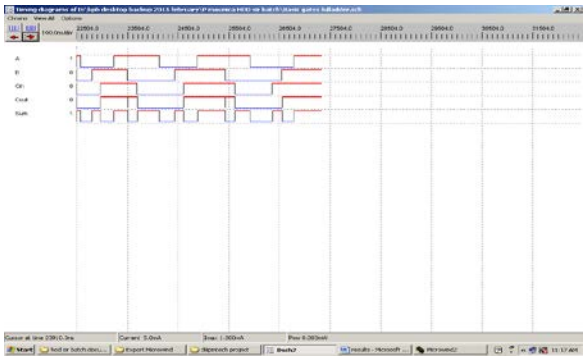
1. Introduction:

Adder is the crucial block in ALU. Conventional full adder is as shown below, it uses basic AND,EXOR, OR gates for SUM and CARRY.

Full adder using gates



Timing diagram of full adder using gates



ISSN 2348 – 7968

Basic CMOS Full Adder

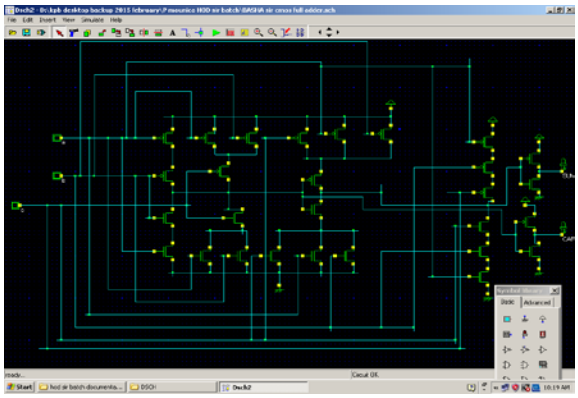


Fig1: cmos full adder

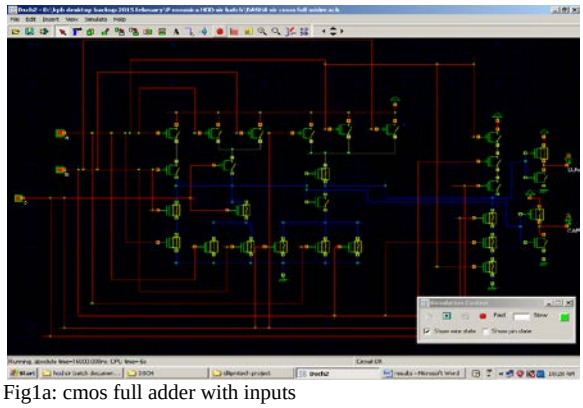


Fig1a: cmos full adder with inputs

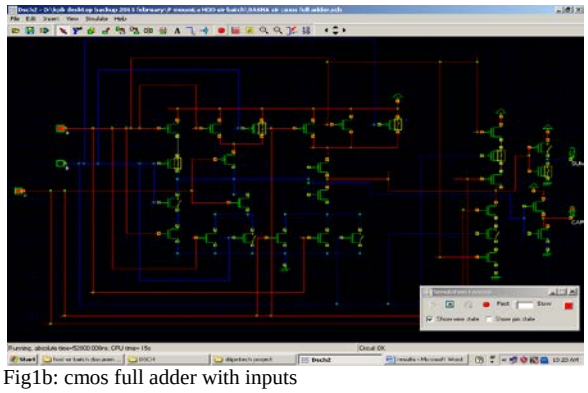


Fig1b: cmos full adder with inputs

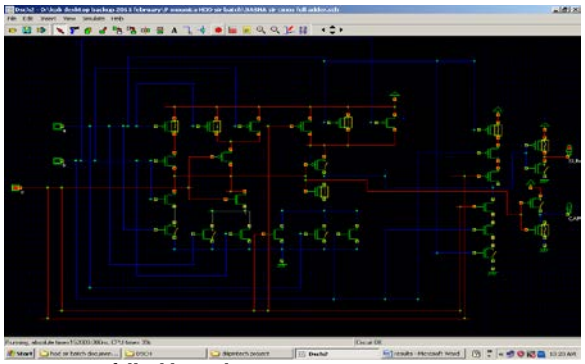


Fig1c: cmos full adder with inputs

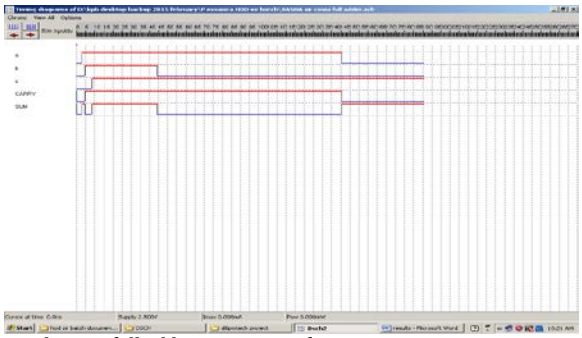


Fig1d: cmos full adder timing waveform

With the rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts [7]-[10]. The role of power dissipation in VLSI systems is pervasive. For high performance design, power dissipation can be the limiting factor to clock speed and circuit density because of the inability to get power to circuits or to remove the heat that they generate. For portable information systems, power dissipation has a direct bearing on size ,weight, cost, and battery life. Consequently, power dissipation is becoming widely recognized as a top-priority issue for VLSI circuit design. The challenge facing the VLSI designer is to find and effectively apply circuit techniques that can balance the needs for performance with those of power dissipation [11]. Therefore ultra low power circuits design becomes the major candidate for portable applications such as wireless sensor nodes. One common technique for reducing power is power supply scaling. For CMOS circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss somewhat but results in increased leakages [12].Other techniques used in low power design

ISSN 2348 – 7968

include clock gating and dynamic voltage/frequency scaling.

Sub threshold circuit design involves scaling the supply voltage below the threshold voltage, where load capacitances are charged/discharged by sub threshold leakage currents. Leakage currents are orders of magnitude lower than drain currents in the strong inversion regime, therefore there is a significant limit on the maximum performance of subthreshold circuits. Therefore, traditionally, subthreshold circuits have been used for applications which require ultra-low power dissipation, with low-to-moderate circuit performance [5].In the first part of this chapter, different topologies for full-adders are presented along with some circuit modifications to reduce the power consumption. Due to the importance of leakage power consumption in digital CMOS circuits, new technique is proposed to reduce the sub-threshold leakage current in high fan-in gates (e.g. OR gate) and basic block like as compressors for high-performance applications.

Energy-efficiency is one of the most required features for modern electronic systems designed for high-performance and/or portable applications. In one hand, the ever increasing market segment of portable electronic devices demands the availability of low-power building blocks that enable the implementation of long-lasting battery-operated systems. On the other hand, the general trend of increasing operating frequencies and circuit complexity, in order to cope with the throughput needed in modern high-performance processing applications, requires the design of very high-speed circuits. The power-delay product (PDP) metric relates the amount of energy spent during the realization of a determined task, and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies, and scenarios. Addition is a fundamental arithmetic operation that is broadly used in many VLSI systems, such as application-specific digital signal processing (DSP) architectures and microprocessors. This module is the core of many arithmetic operations such as addition/subtraction, multiplication, division and address generation. As stated above, the PDP exhibited by the full-adder would affect the system's overall performance [1]. Thus, taking this fact into consideration, the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems. In this paper, we report the design and performance comparison of two full-adder cells implemented with an alternative internal logic structure, based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain balanced delays in SUM and CARRY outputs, respectively, and pass-transistor powerless/groundless logic styles, in order to reduce power consumption. The resultant full-adders show to be more efficient on regards of power consumption and delay when compared with other ones reported previously as good candidates to build low-power arithmetic modules.

2. For low power circuit implementation various reduction are as follows:

Clock frequency reduction

Reducing the clock frequency is not as beneficial as reducing the supply voltage. However, many processors of today have different power-down modes where the clock signal is silenced to blocks of the application that are not used at the moment. This is referred to as clock gating. Clock gating can in most cases be used in conjunction with other low-power techniques.

Switched capacitance reduction

Capacitive load, originating from transistor capacitances (gate and diffusion) and interconnect wiring, is to be minimized. This is achieved by having as few transistors and circuit nodes as possible, and by reducing transistor sizes to a minimum. In particular, the number of (high capacitive) inter-cell connections and their length (influenced by the circuit size) should be kept minimal. Transistor downsizing is an effective way to reduce switched capacitance of logic gates on noncritical signal paths. For that purpose, a logic style should be robust against transistor downsizing,

ISSN 2348 – 7968

i.e., correct functioning of logic gates with minimal or near-minimal transistor sizes must be guaranteed.

Supply voltage reduction

Reducing the supply voltage is an attractive solution to reduce the power consumption since both the switched and the short-circuit power consumption have a strong VDD dependence. There are however some drawbacks with this method:A lower VDD causes longer delays.

There is an overhead in generating another lower VDD on chip.The supply voltage in state-of-the-art processes is already very low, which does not leave much margin to play with.A delay penalty can be mitigated by reducing the threshold voltage but then the subthreshold leakage will increase exponentially. The supply voltage and the choice of logic style are indirectly related through delay driven voltage scaling [28]. That is, a logic style providing fast logic gates to speed up critical signal paths allows a reduction of the supply voltage in order to achieve a given throughput. For that purpose, a logic style must be robust against supply voltage reduction, i.e., performance and correct functioning of gates must be guaranteed at low voltages as well. This becomes a severe problem at very low voltages of around 1 V and lower, where noise margins become critical.

Switching activity reduction

Switching activity of a circuit is predominantly controlled at the architectural and registers transfer level (RTL). At the circuit level, large differences are primarily observed between static and dynamic logic styles. On the other hand, only minor transition activity variations are observed among different static logic styles and among logic gates of different complexity, also if glitching is concerned. To reduce the power consumption Gray code can be one solution since in this code only flip one bit between consecutive numbers. Activity-based decomposition is another activity-based reduction technique

Short-circuit current reduction: Short-circuit may vary by a considerable amount between different logic styles. They also strongly depend on input signal slopes (i.e., steep and balanced signal slopes are better) and thus on transistor sizing. Their contribution to the overall power consumption is rather limited but still not negligible (10–30%), except for very low voltages. A low power logic style should have minimal short-circuit currents and of course, no static currents besides the inherent CMOS leakage currents.

3. Outputs

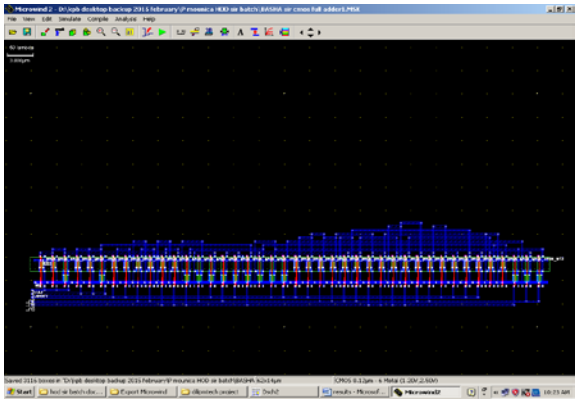


Fig1e: cmos full adder layout

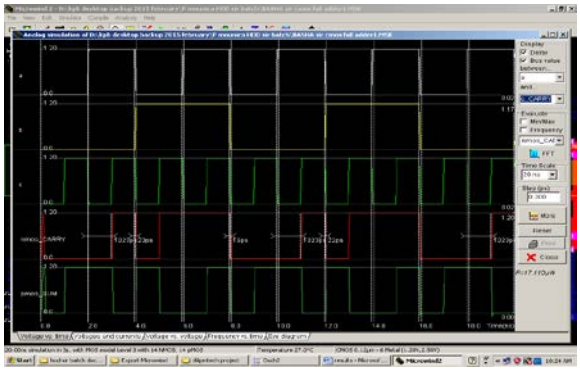
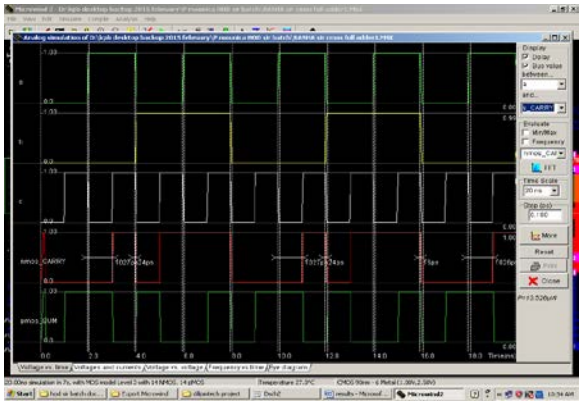


Fig1f: Analog Simulation of cmos full adder of 120nm technology



ISSN 2348 – 7968

Fig1g: Analog Simulation of cmos full adder of 90nm technology

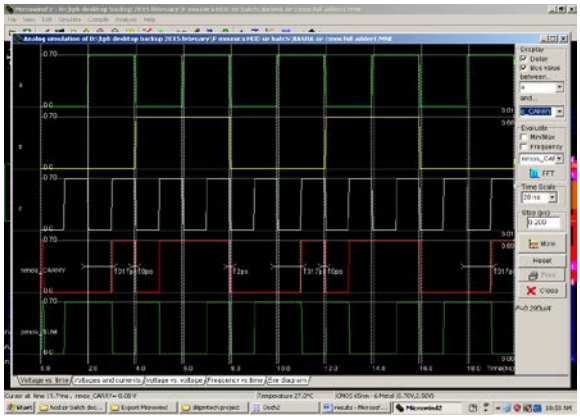


Fig1h: Analog Simulation of cmos full adder of 65nm technology

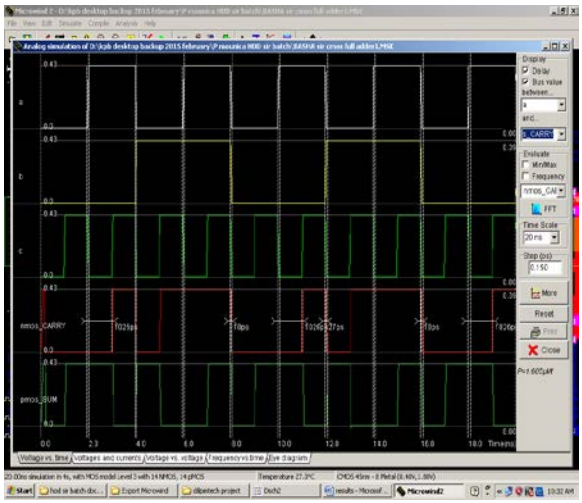


Fig1i: Analog Simulation of cmos full adder of 45nm technology

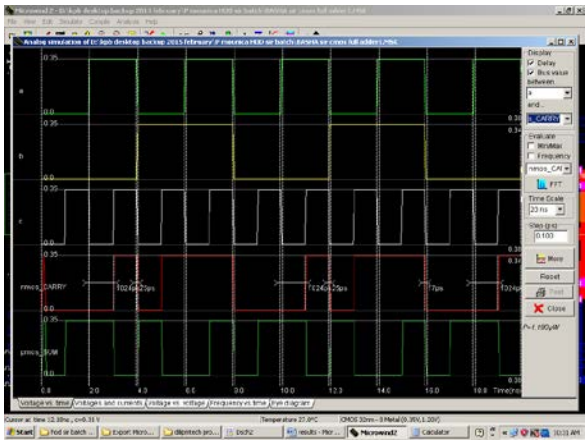


Fig1j: Analog Simulation of cmos full adder of 32nm technology

Results Table for CMOS full adder

S.NO	*Foundry-Technology*	*No. of Metals*	*Power Dissipation*
1	120nm	6	17.110µW
2	90nm	6	13.526 µW
3	65nm	6	6.295µW
4	45nm	8	1.605µW
5	32nm	8	1.190µW

When compared with various foundry technologies like 120nm.90nm,65nm,45nm, from the above table we can conclude that CMOS full adder with 32nm is having low power dissipation.

COMPRESSORS:

4by2compressor

Fig2: 4 by 2 compressor

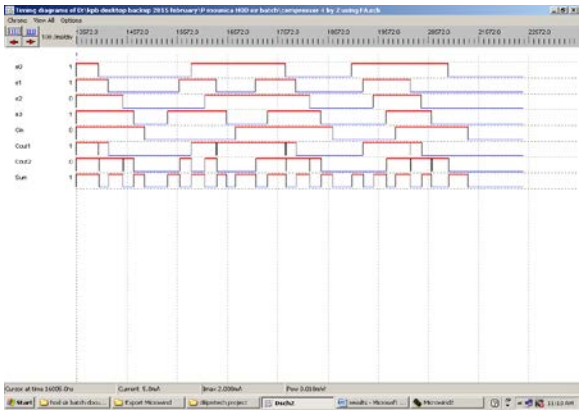


Fig2a: timing diagram of 4 by 2 compressor

ISSN 2348 – 7968

Layout of 4 by 2 compressor

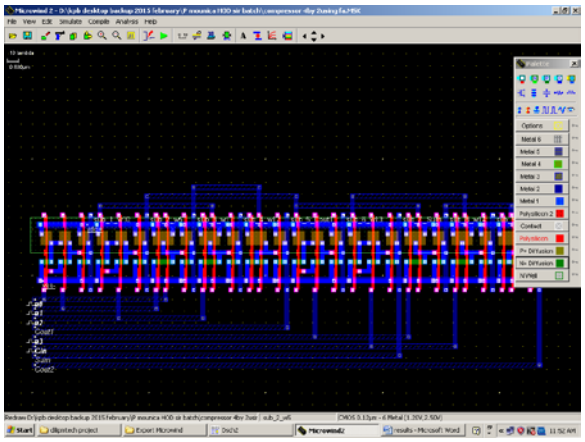


Fig2b: Layout of 4 by 2 compressor

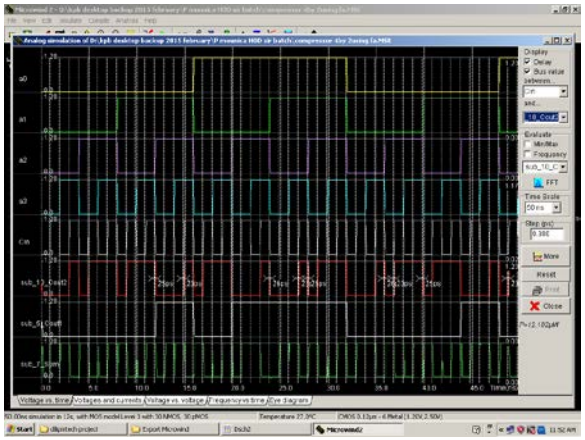


Fig2c: Analog simulation of 4 by 2 compressor of 120 nm technology

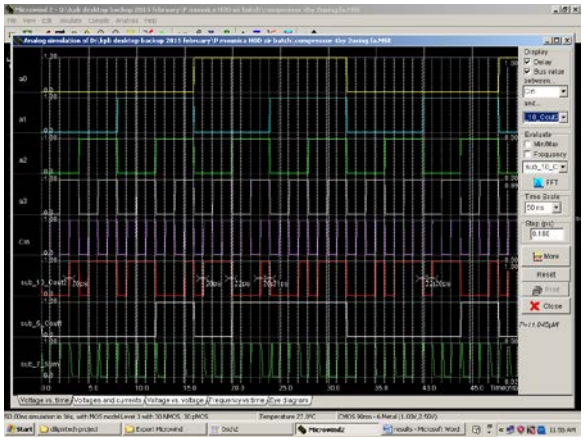


Fig2d: Analog simulation of 4 by 2 compressor of 90 nm technology

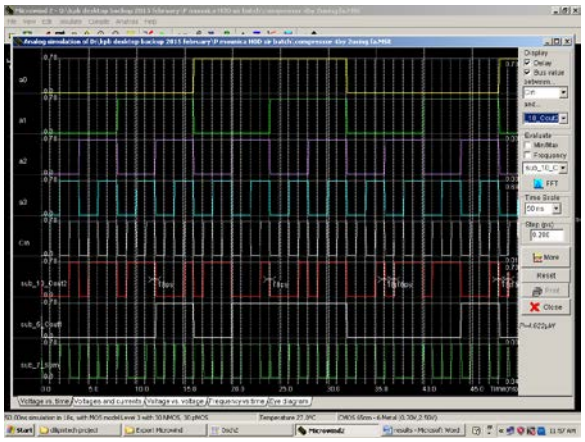


Fig2e: Analog simulation of 4 by 2 compressor of 65 nm technology

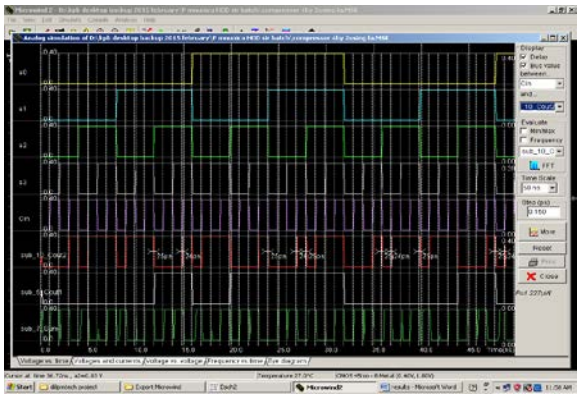


Fig2f: Analog simulation of 4 by 2 compressor of 45 nm technology

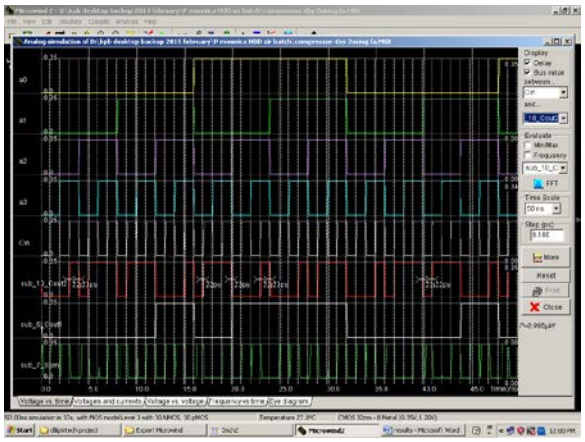


Fig2g: Analog simulation of 4 by 2 compressor of 32 nm technology

ISSN 2348 – 7968

Results Table for 4 by 2 compressor

S.NO	*Foundry-Technology*	*No. of Metals*	*Power Dissipation*
1	120nm	6	12.182µW
2	90nm	6	11.045 µW
3	65nm	6	4.622µW
4	45nm	8	1.227µW
5	32nm	8	0.99µW

When compared with various foundry technologies like 120nm.90nm,65nm,45nm, from the above table we can conclude that 4 by 2 compressor with 32nm is having low power dissipation.

5by2 compressor

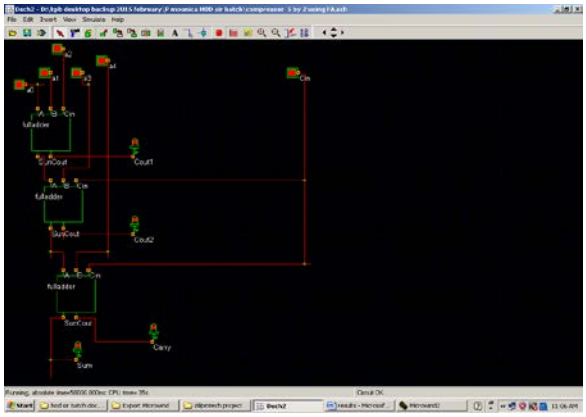


Fig3: 5 by 2 compressor

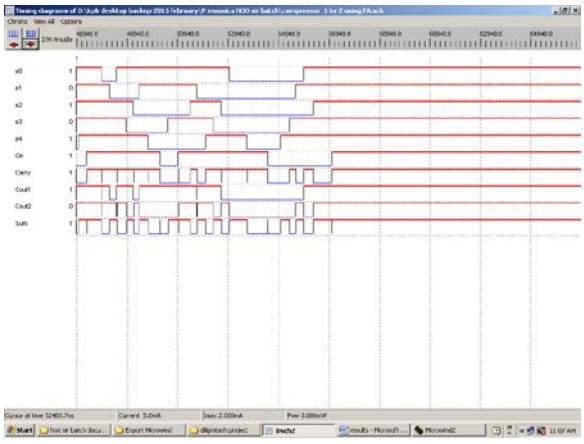


Fig3a: timing diagram of 5 by 2 compressor

Layout of 5 by 2 compressor

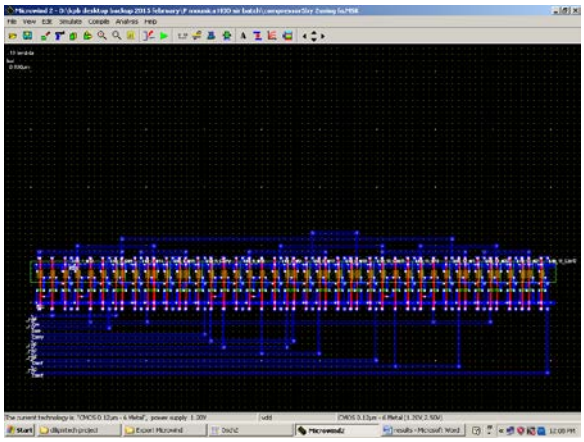


Fig3b: Layout of 5 by 2 compressor

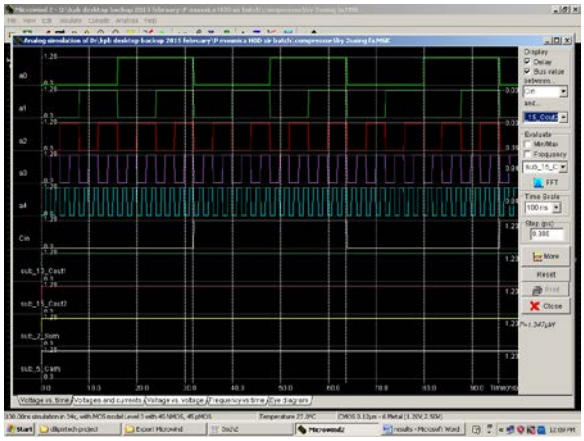


Fig3c: Analog simulation of 5 by 2 compressor of 120 nm technology

7 by 2 compressor

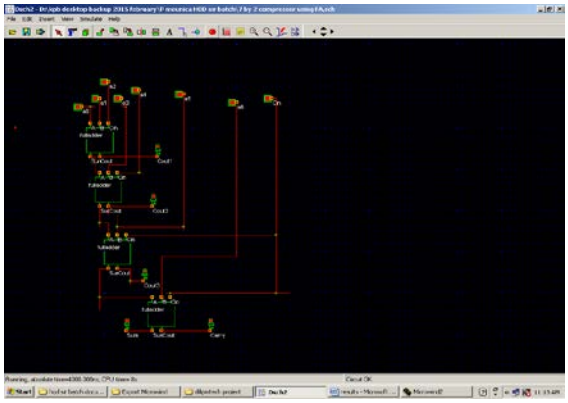


Fig4: 7 by 2 compressor

ISSN 2348 – 7968

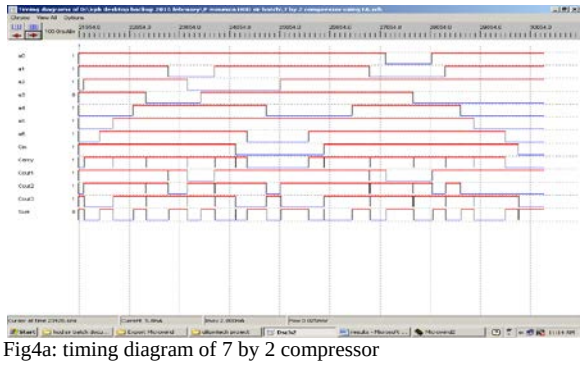


Fig4a: timing diagram of 7 by 2 compressor

Layout of 7 by 2 compressor

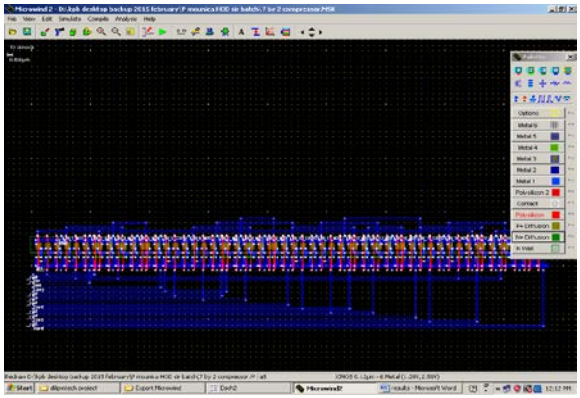


Fig4b: Layout of 7 by 2 compressor

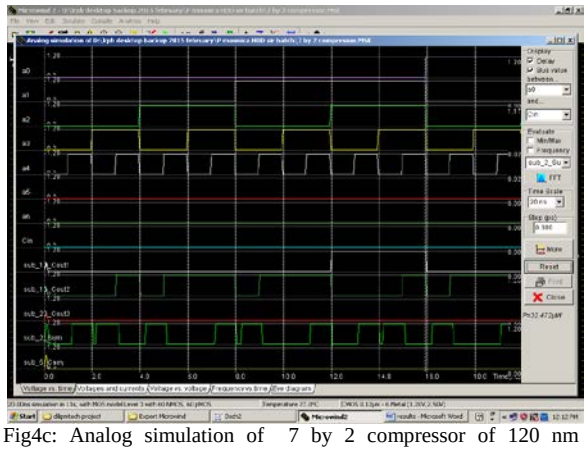


Fig4c: Analog simulation of 7 by 2 compressor of 120 nm technology

SERF:

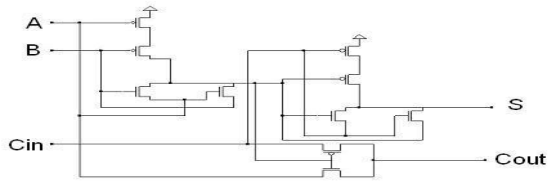
The Static Energy Recovery Full Adder (SERF) uses only 10 transistors to implement the full adder function. The design was inspired by the XNOR gate full adder design. ..In non-energy recovery design the charge applied to the load capacitance during the logic level high is drained to ground during logic level low[10]. It should be noted that the new SERF adder has no direct path to the ground. The elimination of a path to ground reduces power consumption, removing the short circuit from the power equation. The charge stored at the load capacitance is reapplied to the control gates, the combination of not having a direct path to ground and re-application of the load charge to the control gate makes the energy – recovering full adder an energy efficient design but it has the threshold loss problem

working of SERF full adder:

SERF design uses only 10 transistors to implement a full adder.This circuit operates well at higher supply voltages, but if the supply voltage is scaled to voltages lower than 0.3V, this circuit fails to work. Table 1 shows the SERF operation with different input signals. As it can be seen, the SERF adder (Figure.3.1) is confronted with serious problems especially at lower supply voltages. Assume that one of the two input vectors ABCin=“110” and “111” are applied. As seen from Fig 3.1, when A=1 and B=1, the F node voltage is Vdd-Vth. Now if Cin=0 then Cout will be equal to Vdd-2Vth and the Sum signal is going to zero driven by a MOS transistor with its gate connected to Vdd-Vth. When Cin=1, Cout is connected to VDD (may be lower) and the SUM signal will go to Vdd-Vth. Another problem with this design is when the floating node is connected to 0 (A=0, B=1 or A=1,B=0).When Cin is “1”, Cout is charged to Vdd, but when Cin=0, Cout must be discharged to ground using a PMOS pass transistor that cannot fully discharge the output. In this case, Cout is discharged to Vtp which is higher than Vtn[11].

This problem is intensified if the circuit works at sub threshold voltage. If A is at logic “1”, some current leaks to the Cout node which makes Cout to increase even more than Vtp in some cases depending on the sizing of the pass transistors. In this case the Sum value is dependent on the Cin state, for instance, if Cin is “1”, the Sum output is going to Vdd-Vth which is a problem in sub threshold region.

ISSN 2348 – 7968



SERF full adder

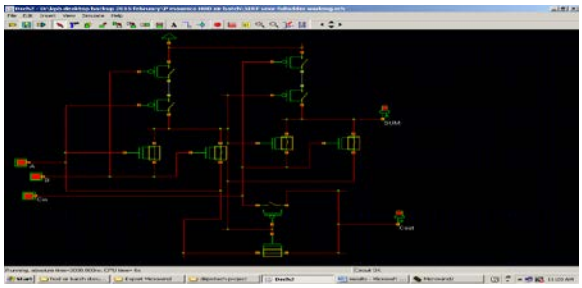


Fig5: SERF XNOR full adder

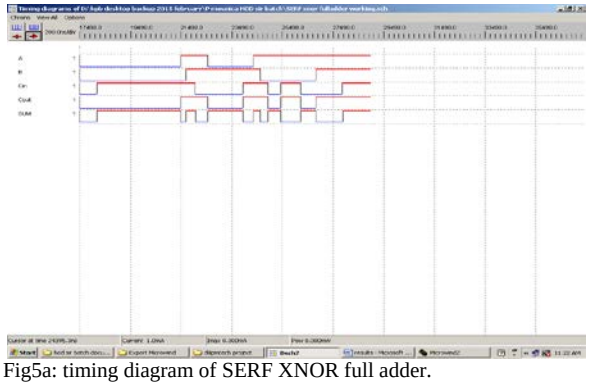


Fig5a: timing diagram of SERF XNOR full adder.

Layout of SERF xnor full adder

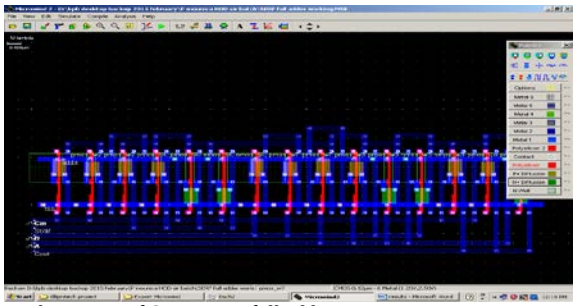


Fig5b: Layout of SERF xnor full adder

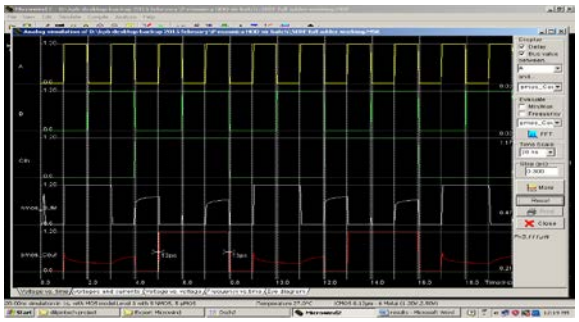


fig 5c:Analog simulation of SERF xnor full adder of 120 nm technology

Modified SERF

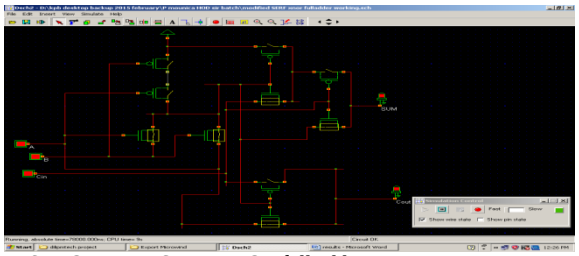


Fig6: MODIFIED SERF XNOR full adder

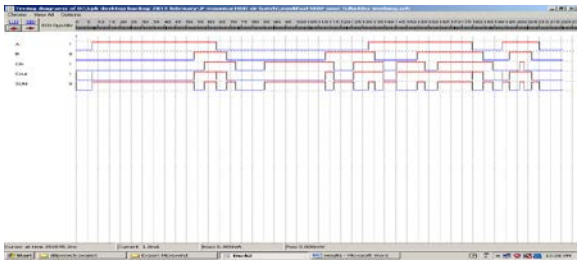


Fig6a: Timing diagram of modified fulladder

Layout of modified serf full adder

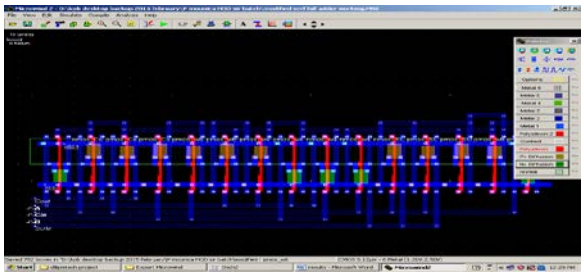


Fig6b: Layout of modified serf full adder

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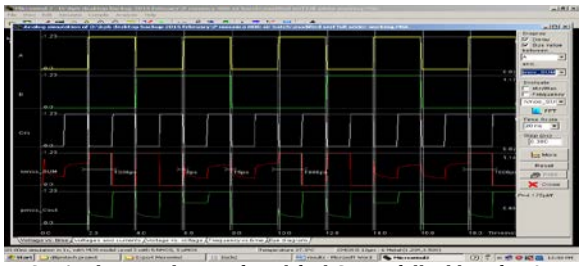

Fig6c: Analog simulation of modified SERF full adder of 120 nm technology

Results table of SERF adder

SERF type	***Foundry-technology***	***NO. Of Metals***	***Power Dissipation***
SERF xnor full adder	120nm	6	5.111µW
Modified SERDF xnor full adder	120nm	6	4.175µW

4. CONCLUSION & FUTURESCOPE

From the above table we conclude that modified serf xnor full adder is dissipating less power when compared with serf xnor full adder. Still low power design can be done without degradation of operation of modified serf, by using various foundry technologies.

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