

Optimization of Fir Filters using MCM and CSE Techniques

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Abstract

The Finite Impulse Response (FIR) filter is a digital filter widely used in Digital Signal Processing applications in various fields like imaging, instrumentation, communications, etc. However, in realizing a large-order filter many complex computations are needed which affects the performance of the common digital signal processors in terms of Area, Power, speed, cost, flexibility, etc. Multiple Constant Multiplication (MCM) and Common Sub expression Elimination (CSE) techniques are extremely effective to improve overall system performance. The FIR filter implementation using MCM and CSE techniques reduce the Area of filter by reducing the number of operators.

In this paper, FIR filter is implemented using MCM and CSE techniques. Direct-form approach in realizing a digital filter is considered. MCM and CSE approach gives a better performance than the common filter structures in terms of speed of operation, cost, and power consumption in real-time. The FIR filter simulated with the help of Xilinx ISE (Integrated Software Environment) 14.5.

For the realization of FIR filter using direct form, FDA (Filter Design and Analysis) tool can also be used. For an N order filter the number of shift register and adders required is N and the number of multipliers required is N+1 in direct form. These filters can work in real time.

Keywords: MCM, CSE, CSD, FIR, IIR, BSE

1. INTRODUCTION

1.1 Filter: Filtering plays an important role in digital signal processing. The process of filtering is widely used in a number of electronic devices to remove a part of signal that damages the signal [16]. The following is the diagram of filter which gives the basic information:-



Figure 1: Block diagram of Filter

A Filter is a network which can change the wave shape, amplitude, phase, frequency and other characteristics of the signal in a desired manner. The main purpose of using the filter in digital signal processing is to improve the quality of a signal by reducing noise, to extract or to combine the desired portion of signal [17].

Filters are used for two purposes: one for separation of signal and for restoration of signal. Signals which are damaged by interference and noise require different techniques to get noiseless signal. A device is used to measure the electrical activity of heart of a baby inside the mother's womb will be damaged by breath and heartbeat signal of the mother. Filters are used at that time to separate the signals and to analyze them individually. When the signal gets corrupted, then restoration of signal is used [16].

Recording of Audio signal which is made with poor equipment is filtered to give the better sound signal output than the originally it produced. When filters are implemented, the coefficient multiplier is the most complex and the slowest component. The cost of implementation of an FIR filter can be reduced by decreasing the complexity of the coefficients.

1.2 Types of Digital Filter: There are two types of digital filters in digital signal processing: one is Finite Impulse Response (FIR) and other is Infinite Impulse Response (IIR).

1.2.1 Finite impulse Response (FIR)

Finite Impulse Response (FIR) digital filter is mostly used in digital signal processing (DSP) applications that are speech processing, loud speaker equalization, echo cancellation, adaptive noise cancellation and various communication applications. FIR means "Finite Impulse Response". If an impulse is given to filter which is a single "one (1)" sample followed by number of "zero (0)" samples then zeroes will come out after "one (1)" sample which makes the way through the delay line of the filter. So FIR filter has finite duration impulse response because it settles to zero in finite time. These filters have no feedback

and are inherently stable [18]. FIR filters are linear phase filters. There is a condition needed to achieve the Linear Phase. The condition is when the filter's phase response is a linear function of frequency, which results in the delay through the filter is same at all frequencies. Thus the filter does not create any type of "phase distortion" or "delay distortion".

A FIR filter is linear phase if the coefficients of a filter are symmetrical around the centre coefficient. It means that first coefficient is same as the last coefficient. Similarly the second coefficient is same as the next to last. Therefore filter should have odd number of coefficients because a single coefficient which is at centre has no mate. FIR filters have great flexibility in shaping their magnitude response. The following is the block diagram of FIR filter which gives the basic idea:-

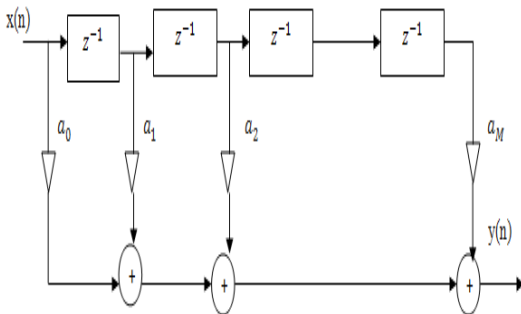


Figure 2: A direct form of FIR Filter

For a FIR filter of order M, each value of the output sequence is the weighted sum of the most recent

input values:-

$$y(n) = a_0x[n] + a_1x[n-1] + \dots + a_Mx[n-M]$$

$$= \sum_{i=0}^M a_i x[n-i] \quad (1)$$

Where,

x[n] is the input signal,

y[n] is the output signal,

M is the order of filter

a_i is coefficient of filter.

FIR filters are known as non recursive filters because filter output does not depend on previous output.

1.2.2. Infinite Impulse Response (IIR) "IIR" means Infinite Impulse Response. If an impulse is applied to

filter which is a single "one (1)" sample followed by number of "zero (0)" samples then an infinite number of non-zero values will be come out. Filter's impulse response will be infinite because of the presence of feedback in the IIR filter [19]. The following is the diagram of IIR filter which gives the basic idea:

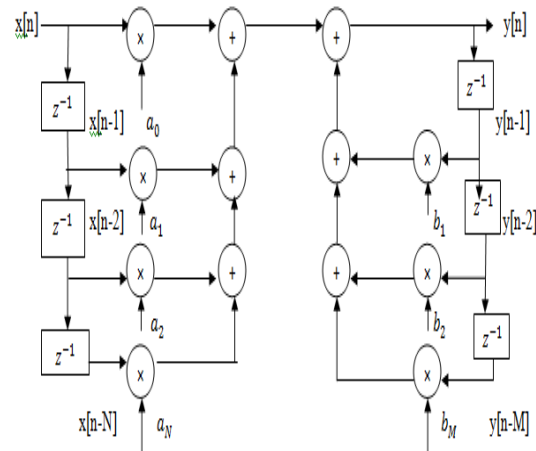


Figure 3: A direct form of IIR Filter

For a IIR filter, each value of the output sequence is:-

$$y[n] = \sum_{i=0}^N a_i x[n-i] - \sum_{j=1}^M b_j y[n-j]$$

Where x[n] is input signal, y[n] is output signal, M is the order of feedback filter, N is the order of feedforward filter, a_N is coefficients of feedforward filter and b_M is coefficients of feedback filter.

2. OPTIMIZATION OF FILTERS

FIR filters are inherently stable and require no feedback. Major factors that influence choice of a specific realization of filter are computational complexity, requirement of memory and finite word length effects. Filter optimization is the process of designing a signal processing filter that satisfies a set of requirements. The purpose for the optimization of the filter is to acquire each of the requirement to make the filter efficient stable and useful. Optimization of FIR filters are done by reducing the area, delay etc by using different algorithm. Area of a filter is reduced by minimizing the number of addition/subtraction operators. This can be only done by using Multiple Constant Multiplication (MCM)

and Common Sub expression Elimination (CSE) Techniques [20]. The multiple constant multiplication (MCM) is defined as a technique to find out the minimum number of adders and subtractors required for the multiplication of multiple constants by an input variable. The CSE is defined as a technique to find out the minimum number of addition and subtraction operators by taking operators as common [21].

3. Literature Survey

There is a lot of work that has been done in the field of FIR filters. There is a lot of work has been done in this field by using different techniques and motives to provide the best system. Researchers have used the different techniques and parameters to provide the best output and performance in any situation. The literature survey of different researchers has been given below:-

Michael A.Soderstrand et al. (2000) in [1] proposed a hardware optimization technique based on minimum adder Canonical Signed Digit (CSD) multiplier blocks is combined with a technique for trading adders to reduce hardware requirements for FIR filter coefficients. Noise free filters can only be achieved using FIR filters because FIR filters can always designed by using sufficient number of bits in the multipliers that rounding or truncation after multiply is not necessary. Thus an idea is carried out by increasing the filter order and decreasing the bits to minimize the hardware requirement. This technique is implemented in Field Programmable Gate Array (FPGA) which is an integrated circuit and it requires high cost.

J. Yli-Kaakinen and T. Saramaki (2001) in [2] have proposed a systematic Multiple Constant Multiplication (MCM) algorithm that minimizes a number of adders to implement an overall filter to meet amplitude criteria. This algorithm performed in two steps: First a Linear Programming algorithm is used to determine the parameter space of coefficients of filter. Second step involves finding the filter parameters to meet amplitude criteria. In this algorithm, it's very difficult to maintain the amplitude. Small change in amplitude will create quantization error which affects the performance of FIR filter.

Paulo Flores et al. (2005) in [3] represented an exact algorithm which helps to maximize the sharing of partial terms in Multiple Constant Multiplication (MCM) technique. They model a Boolean Network which takes all possible partial terms by using AND and OR gates. An AND gate represents as an adder or a subtractor. The output of AND gates is summed by OR gates. This algorithm uses binary and Canonical Signed Digit (CSD) representations to represent the

coefficients. Converting coefficients into Binary form, shifting and adding the partials and then converting into Canonical Signed Digit (CSD) will be more complex and take more time to represent a coefficient.

S.Vijay et al. (2007) in [4] represented the complexity of Finite Impulse Response (FIR) filters and reduced by using number of adders and subtractors for implementation of coefficient multipliers. A Common Sub expression Elimination (CSE) algorithm with a based on the Canonic Signed Digit (CSD) representation of coefficients of filter for implementing low complexity FIR filters. In Common Sub Expression Elimination (CSE), first write the expression in binary form. According to bit position, shift the variable and added up the shifted variable. Then maximizes grouping of the sub expressions for the reduction of operators. Canonical signed digits used where there is occurrence of consecutive non zero digits. Steps of converting a binary number into canonical digits repeated again and again until there is no consecutive non zero digits. Thus it's very difficult to deal with canonical signed digits.

Oscar Gustafsson (2007) in [5] has represented Multiple constant multiplication (MCM), realizing a number of constant multiplications using a minimum number of adders and subtractors. An adder graph type algorithm for solving the MCM problem was introduced. In MCM, multiplication of each constant was done by using addition, subtraction and shift operators. In MCM, first write expression in binary form. According to bit position, shift variable and added up the shifted variable. In Adder Graph, adding and shifting and random grouping of sub expressions is used to reduce the number of operators. By using MCM with Adder graph, numbers of operators are reduced but there is no rule to common the block to reduce the number of operators.

R.Mahesh and A.P.Vinod (2008) in [6] have represented the Common Sub expression Elimination (CSE) technique which is based on Canonical Signed Digit Coefficients (CSD). With the help of these, the number of operators can be reduced to realize the multipliers when the filter coefficients are represented in binary form. The reduction of operators can be achieved from this method but this is only for short filters. If there is large number of coefficients in a filter then it creates difficulty to represent coefficients in Canonical Signed Digit form. Because method to represent the coefficients into CSD form is very long.

Mustafa Aktan et al. (2008) in [7] proposed an algorithm to design a low power and hardware

efficient Finite Impulse Response (FIR) having a linear phase. This algorithm finds the coefficients of filter with reduced number of signed power of two terms. In this algorithm, fix a coefficient up to a certain value which is determined by the coefficient's boundary values using linear programming. This algorithm requires less number of operators and consumes less power. But this algorithm is used only when there is odd number of coefficients to fulfill the condition of linear phase Finite Impulse Response (FIR).

Levent Aksoy et al. (2008) in [8] have represented an exact Common Sub expression Elimination (CSE) for sharing terms in Multiple Constant Multiplication (MCM). This algorithm deals with the Boolean networks to cover the all terms which generate the set of coefficients in Multiple Constant Multiplication (MCM). Linear Programming is used to reduce the number of gates used in it. This algorithm handles the binary and Canonical Signed Digits (CSD) representations for the coefficients. This paper results the reducing in delay but area of filter is increased. So this algorithm is not efficient to decrease the number of operators.

Chip-Hong Chang et al. (2008) in [9] have presented a new methodology to reduce the number of operators in Finite Impulse Response (FIR) digital filters. An adder graph like data structure called Multiroot Binary Partition Graph (MBPG) in which a set of coefficients is partitioned into symbols for the common sub expression elimination. A minimum number of different pairs or group of symbols can be used to code a set of coefficients based on their probability and conditional probability of occurrence. This algorithm will reduce the critical path delay, complexity of a filter and consume power. But this algorithm will be lengthy for high order finite impulse response filters.

Mathias Faust and Chip-Hong Chang (2009) in [10] were proposed Transposed Direct form of FIR filter instead of simple Direct form of FIR filter to optimize the coefficients by reducing the number of operators in Multiple Constant Multiplication (MCM) technique. Transposed Direct form is used over Direct form because of its shortest path delay. In Direct form, input is delayed before the coefficient multiplication. In Transposed direct form, sum generated by the outputs of coefficient multiplier, are delayed. So large numbers of registers are required in Transposed direct form. The delay through the structural adders is reduced except last tap. The one full adder delay increased for the last tap which will be tolerable and will not affect the performance of a filter. Area of filter reduced by reducing the delays through structural adders but require more number of

registers. Thus there is tradeoff between Area of filter and Cost of Filter.

Guifeng Liu et al. (2010) in [11] have represented an approach to reduce the quantization noise in Multiple Constant Multiplication (MCM) while maintaining the performance and reduce the area of filter. In Multiple Constant Multiplication (MCM), some of information is lost called round off noise due to the presence of adders and subtractors. But the shifts do not contribute to any noise because they are realized using wiring. To reduce the round off noise, add more bits to the appropriate nodes. When numbers of bits are added to the nodes of Multiple Constant Multiplication (MCM) block then quantization noise will be decrease but there is increase in area of filter. More bits means more accuracy and more space is used. Thus there is effectively tradeoff between filter performance and implementation area.

Kenny Johansson et al. (2011) in [12] have represented a graph based minimum adder depth algorithm for Multiple Constant Multiplication (MCM) technique which reduces the area of filter and power. If adder depth will low then efficient area of filter and power consumption can be done. This algorithm uses shift operators, adders/subtractors operators and graph adders to reduce the power and Area of filter. Graph based algorithm is efficient algorithm to get low adder depth but it is not used for Cascaded adders because they have large adder depth. The number of cascaded adders strongly effects the power consumption.

L.Aksoy et al. (2013) in [13] have represented the design of low complexity using bit-parallel multiple constant multiplications (MCM) operation which reduces the complexity of many digital signal processing systems. In digital-serial design, input data is divided into the number of bits. Then it processed the data serially bit by bit but applies each bit in parallel. Digital-serial computation plays an important role when bit serial implementations can't meet the delay requirements then bits sends in parallel need more hardware. FIR filters which are under the shifts-adds architecture having significant area reduction as compared to that filter design which is implemented by using digital serial constant multiplier. Some attention had been given to the digit-serial MCM design which offers low complexity MCM operation at the cost of an increased delay. Thus it was a tradeoff between time and Area of filter.

Firas Al-Hasani et al. (2013) in [14] have represented Common Sub expression Elimination (CSE) algorithm which is used to minimize the complexity of the Multiple Constant Multiplication

(MCM) operation. Multiple constant multiplications used Binary Signed Digit (BSD) number system to design the coefficients. The Binary signed digits (BSD) used in this paper which gives a better performance over Canonical Signed Digits (CSD). BSD representation is used to find the possible decompositions which results the possibility of finding MCM realizations with minimum logic depth is increased because the sub expression space becomes large. In BSD, first a decimal number is converted into binary digits. Each digit associated with a sign, positive or negative. So a decimal number can be represented in many ways using Binary Signed Digits. Thus BSD show redundancy.

Levent Aksoy et al. (2014) in [15] have represented Multiple Constant Multiplication (MCM) which realizes the multiplication of constants by a variable. It can be implemented by using generic multipliers and adders/sub tractors. This algorithm is implemented by Field Programmable Gate Arrays (FPGA) using Linear Programming Formulation and Graph Based algorithm. The use of Multiple Constant Multiplication (MCM) design leads to FIR filter design requiring less number of operators, having less delay and consuming less power with respect to those include only adders/sub tractors. But due to the further use of large number of algorithms this becomes more complex.

4. Multiple Constant Multiplications (MCM)

Existing optimization algorithms for the multiplier less realization of multiple constant multiplications (MCM) typically target the minimization of the number of addition and subtraction operations [23]. Multiple constant multiplication (MCM) is defined as a technique to find out the minimum number of addition/subtraction operations required for the multiplication of multiple constants by an input variable [24]. Multiplier Constant Multiplications is a straight forward way of realizing the constant multiplications under a shift-adds architecture. It is first to define the constants under a particular number representation, and second, for the nonzero digits in the representation of the constant, is to shift the input variable according to the digit positions and add/subtract the shifted variable with respect to the digit values [25]. Taking a simple example, consider the constant multiplications $29x$ and $43x$ [26]. Their decompositions in MCM are listed as follows

$$29x = (11101)_{bin}x = x \ll x + 2 \ll x + 3 \ll x + 4 \quad (iii)$$

$$43x = (101011)_{bin}x = x \ll x + 5 \ll x + 3 \ll x + 1 \quad (iv)$$

These coefficients are implemented as follows using Multiple Constant Multiplication (MCM):

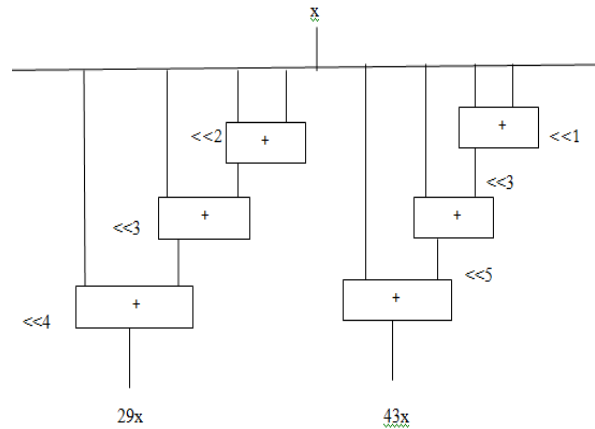


Figure4: Implementation of coefficients in MCM form

In this, x is input signal. “<<” sign represents the shifting of variable. It shifts the variable by two raised to the power. In this MCM technique only six adders are used to implement two coefficients instead of using a number of multipliers. However, the sharing of common partial products in the shift adds architecture allows for large reductions in the number of operations and also reduction in area and power dissipation of the MCM designs [22].

5. Common Sub expression Elimination (CSE)

A Common Sub Expression Elimination (CSE) technique is advanced technique of Multiple Constant Multiplication (MCM) in which maximum sharing of variable is done to reduce the number of operators so that area of filter can be reduced. Common Sub expression Elimination technique is simply a shifting and adding of variable to implement the coefficients. First a decimal number is converted into binary form. Shift the input variable according to the digit position and then add/subtract the shift variable according to the coefficient value. It can be explained clearly by taking the same example as in Multiple Constant Multiplication (MCM) technique. Taking a simple example, consider the constant multiplications $29x$ and $43x$ [26]. Their decompositions in CSE are listed as follows

$$29x = (11101)_{bin}x = x \ll x + 2 \ll x + 3 \ll x + 4 \quad (v)$$

$$43x = (101011)_{bin}x = x \ll x + 5 \ll x + 3 \ll x + 1 \quad (vi)$$

In above, 11 and 101 both are used for sharing of variables. Both numbers are in binary form. 11 represents 3 in decimal form and 101 represents 5 in decimal form. These coefficients are implemented as follows in Common Sub expression Elimination (CSE):

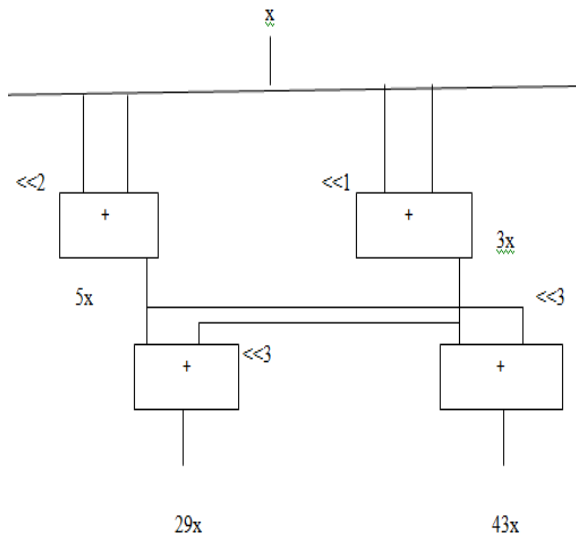


Figure 5: Implementation of coefficients in CSE form [13]

In this, x is input signal. “<<” sign represents the shifting of variable. It shifts the variable by two raised to the power. In this CSE technique only four adders are used to implement two coefficients whereas in Multiple Constant Multiplication (MCM) six adders are used. However, the maximum sharing of common partial products in the shift adds architecture allows for great reductions in the number of operations. Use of sub tractor instead of adders will reduce the cost of FIR filter. Common Sub expression Elimination (CSE) technique gives the efficient decrease in the area of FIR filter which gives the better performance of FIR filter.

6. IMPLEMENTATION

In this, FIR filter is implemented using direct form. FIR filter’s Direct form uses large number of operators which increases the area of filter. In this, different parameters like area, delay and memory requirement are described using Xilinx.

6.1 Device Utilization Summary

Figure 6 describes the device utilization summary. This summary gives the idea about number of operators. It tells that how many operators are available, how many operators are used. Simply this gives the knowledge about area of filter. Area of filter can be finding by count the number of slice flip flops, number of input LUT’s and number of shift registers. Less number of these operators, less will be the area of filter.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	111	1,920	5%
Number of 4 input LUTs	94	1,920	4%
Number of occupied Slices	58	960	6%
Number of Slices containing only related logic	58	58	100%
Number of Slices containing unrelated logic	0	58	0%
Total Number of 4 input LUTs	96	1,920	5%
Number used as logic	93		
Number used as a route-thru	2		
Number used as Shift registers	1		
Number of bonded I/Os	49	66	74%

Figure 6: Device Utilization Summary of FIR filter using direct form

In this, Total 408 operators are used to implement FIR filter using direct form.

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	39	10,944	1%
Number of 4 input LUTs	32	10,944	1%
Number of occupied Slices	23	5,472	1%
Number of Slices containing only related logic	23	23	100%
Number of Slices containing unrelated logic	0	23	0%
Total Number of 4 input LUTs	37	10,944	1%
Number used as logic	32		
Number used as a route-thru	5		
Number of bonded I/Os	21	240	8%

Figure 7: Device Utilization Summary of FIR filter using MCM and CSE

In this, Total 152 operators are used to implement FIR filter using MCM and CSE

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Total memory usage is 278684 kilobytes
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Figure 8: Total memory used by FIR filter using direct form

Figure 8 shows memory used by these operators. Total memory used by operators is 278684 kilobytes

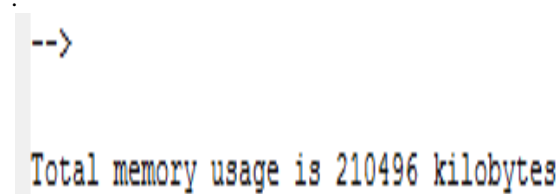


Figure 9: Total memory used by FIR filter using MCM and CSE

6.2 Timing Summary

Figure 8 gives the timing summary. With the help of timing summary, delay and speed of filter can be calculated. If delay will be less then speed will be more. Minimum delay will give the better performance of FIR filter. Delay is calculated in nano seconds. Delay Period of FIR filter is 5.140 ns.

Timing Summary:

Speed Grade: -4

Minimum period: 5.140ns (Maximum Frequency: 194.553MHz)
 Minimum input arrival time before clock: 11.517ns
 Maximum output required time after clock: 4.283ns
 Maximum combinational path delay: No path found

Figure 10: Timing Summary of FIR filter using direct form

Figure 11 gives the timing summary of FIR filter using MCM and CSE. Delay Period of FIR filter is 1.749 ns.

Timing Summary:

Speed Grade: -12

Minimum period: 1.749ns (Maximum Frequency: 571.739MHz)
 Minimum input arrival time before clock: 2.916ns
 Maximum output required time after clock: 3.793ns
 Maximum combinational path delay: No path found

Figure 11: Timing Summary of FIR filter using MCM and CSE

7. COMPARISON OF DIRECT FORM AND MCM, CSE

There is reduction of operators using MCM and CSE for the implementation of FIR filter. Thus the area of filter is reduced using MCM and CSE. Memory used and delay also decrease using MCM and CSE. In table 1, a comparison between direct form and MCM, CSE is given:

Table 1: Detailed dimensions of Direct form, MCM and CSE

Techniques Used	Number of operators	Delay(in nanosecond)	Total Memory Used(in kilobytes)
Direct form	408	5.140	278684
MCM and CSE	152	1.749	210496

8. CONCLUSION

During the last decade, digital communication industry has grown at a very fast rate. With the rapid development of digital communication system, different techniques for the optimization of FIR filters have attracted considerable attention. They are commonly used in digital signal processing system. Due to these reasons the demand for FIR filters has increased. With the advancement of technology, communication devices such as radios in which more noise is present, thus the large number of filters to be used in such devices to remove the noise. Thus the purpose of this thesis work is to analyze and design the optimization techniques to reduce the area of filter, delay and power. So that signal can process at fast rate. A direct form, MCM and CSE techniques for the optimization of FIR filters are presented. Compare to many techniques, these techniques are designed based on a simple structure and suitable for optimization of FIR filters. The proposed techniques are considered to achieve minimum area, delay and power of filter using less number of operators, so it can give fast rate to process a signal. The measured results show that the in case of

Direct form, number of slice flip flops are 111, number of input LUTs are 94 and number of occupied slices are 58. Thus total number of operators used are 408. The minimum period is 5.140 ns. Total memory used by operators used to implement a FIR filter is 278684.

MCM and CSE, number of slice flip flops are 39, number of input LUTs are 32 and number of occupied slices are 23. Thus total number of operators used are 152. The minimum period is 1.749 ns. Total memory used by operators used to implement a FIR filter is 210496.

Thus the reduction of area, delay and power is there when Multiple Constant Multiplication (MCM) and Common Sub expression Elimination (CSE) are used. In addition, the proposed techniques are easily implemented and give a better response of FIR filter. These techniques can be used widely in digital signal processing.

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