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Analysis of grid synchronization methods for three phase distributed power generation systems

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ABSTRACT

In this project, the synchronization of grid voltage of the distributed generation systems are studied by the considering various grid synchronization techniques. In order to get the required amount of accurate and fast grid voltage synchronization algorithms this is important to work under distorted and unbalanced conditions. Therefore it is necessary to analyze the synchronization capability of three advanced synchronization systems: the three-phase enhanced PLL the decoupled double synchronous reference frame phase-locked loop (PLL), and the dual second order generalized integrator PLL which is implemented under such conditions. Moreover if other system depend upon frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq0 controllers. By using MATLAB/Simulink software the simulation have been done.

Index Terms— Electric variable measurements, electrical engineering, frequency estimation, harmonic analysis, monitoring, synchronization, Fuzzy logic controller.

I. INTRODUCTION

The power share of renewable energy-based generation systems is supposed to reach 20% by 2030, where wind and photovoltaic (PV) systems are assumed to be the most outstanding examples of integration of such systems in the electrical network [1].

The increased penetration of these technologies in the electrical network has reinforced the already existing concern among the transmission system operators (TSOs) about their influence in the grid stability; as a consequence, the grid connection standards are becoming more and more restrictive for distribution generation systems in all countries [2]–[6].

In the actual grid code requirements (GCRs), special constraints for the operation of such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand. Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic [7].

Although the LVRT requirements various standards are very different, as shown in [8], the first issue that generation systems must afford when voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel cage induction generators, where the voltage drop in the stator windings can conduct the generator to an over speed tripping, as shown in [9]. Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions [10], [11].Likewise, PV systems would also be affected by the same lack of current controllability.

Solutions based on the development of auxiliary systems, such as STATCOMs and dynamic voltage regulators (DVRs), have played a decisive role in enhancing the fault ride through (FRT) capability of distributed generation systems, as demonstrated in [12]. In any case, a fast detection of the fault contributes to improving the effects of

these solutions; therefore, the synchronization algorithms are crucial.

In certain countries, the TSOs also provide the active/reactive power pattern to be injected into the network during voltage sag; this is the case for the German E-on [2] and the Spanish Red Eléctrica Espanola (REE).

This trend has been followed by the rest of the TSOs; moreover, it is believed that this operation requirement will be extended and specific demands for balanced and unbalanced sags.

These solutions are based on advanced control systems that need to have accurate information of the grid voltage variables in order to work properly, something that has prompted the importance of grid synchronization algorithms. In power systems, the synchronous reference frame PLL (SRF PLL) is the most extended technique for synchronizing with three-phase systems [13]. Nevertheless, despite the fact that the performance of SRFPLL is satisfactory under balanced conditions, its response can be inadequate under unbalanced, faulty, or distorted conditions [14]–[15].

In this work, three improved and advanced grid synchronization systems are studied and evaluated: the decoupled double synchronous reference frame PLL (DDSRF PLL) [16], the dual second order generalized integrator PLL (DSOGI PLL), [17]and the three-phase enhanced PLL (3phEPLL) [18]. Their performance, computational cost, and reliability of the amplitude and phase detection of the positive sequence of the voltage, under unbalanced and distorted situations, have been evaluated according to experimental grid fault patterns extracted from [19] and [20], which have been reproduced in a real scaled electrical network.

II.GRID S YNCHRONIZATION SPECIFICATIONS BASED ON GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on analyzing the individual dynamic performance of each proposal, without first determining a time response window within the dynamic behavior of the system under test, which would be considered to be satisfactory. In this paper, in order to evaluate the response of the grid synchronization topologies under test, a common performance requirement for all the structures has been established in this section, considering the needs that can be derived from the LVRT requirements.

Despite the fact that the detection of the fault can be carried out with simpler algorithms the importance of advanced grid synchronization systems lies in the necessity of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power required by the TSO.

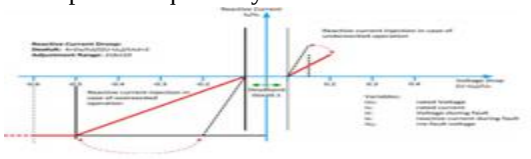

Fig.1. E-on voltage support requirement in the event of grid fault.

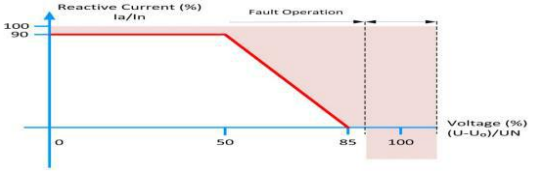

Fig.2. REE voltage support requirement in the event of grid fault

In the German standard, it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the transformer to at least 2% of the rated current for each percent of the voltage dip, as shown in Fig.1. 100% reactive power delivery must be possible, if necessary. A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and be able to inject full reactive power after 150 ms, as shown in Fig. 2.

III. DESCRIPTION OF THE THREE SYNCHRONIZATION S YSTEMS

Many of the positive-sequence detection algorithms are based on SRF PLLs. Despite having a good response under balanced conditions, their performance becomes insufficient in unbalanced faulty grids (95% of cases), and their good operation is highly conditioned to the frequency stability, which is incompatible with the idea of a robust synchronization system.

A. DDSRF PLL

The DDSRF PLL which is implemented for the improving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counter clockwise and another one clockwise, in order to achieve an accurate detection of the positive- and negative-sequence components

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of the grids voltage vector when it is affected by unbalanced grid faults.

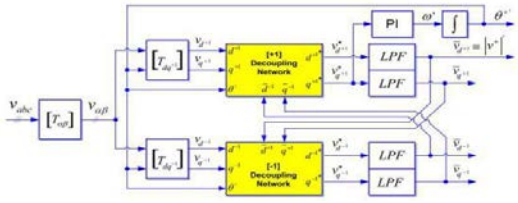

Fig.3. DDSRF-PLL block diagram

In the framework of these topologies, three PLL structures will be discussed and evaluated in this project.

The diagram of the DDSRF PLL is shown in Fig.3. When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a dc voltage on the dq+1 axes of the positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the dq−1 axes of the negative-sequence SRF

Since the amplitude of the oscillation on the positive-sequence SRF matches the dc level on the negative sequence SRF and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters (LPFs) in Fig. 3 are responsible for extracting the dc component from the signal on the decoupled SRF axes

Finally, the PI controller of the DDSRF PLL works on the decoupled q-axis signal of the positive-sequence SRF (v∗q+1) and performs the same function as in an SRF PLL, aligning the positive-sequence voltage with the d-axis. This signal is free of ac components due to the effect of the decoupling networks; the bandwidth of the loop controller can be consequently increased.

B. DSOGI PLL

The operating principle of the DSOGI PLL for estimating the positive- and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the αβ stationary reference frame

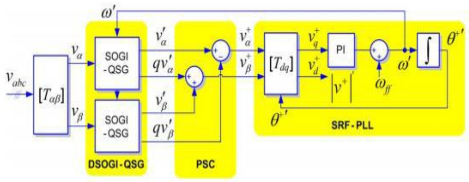

Fig.4. DSOGI-PLL block diagram.

The diagram of the DSOGI PLL is shown in Fig. 4. As it can be noticed, the ISC method is implemented by the positive-sequence calculation block. To apply the ISC method, it is necessary to have a set of signals, v α–v β, representing the input voltage vector on the αβ stationary reference frame together with another set of signals, qvα–qvβ, which are in quadrature and lagged with respect to vα–vβ.

C. 3phEPLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has proven to provide good results in single phase synchronization systems. An EPLL is essentially an adaptive band pass filter, which is able to adjust the cutoff frequency as a function of the input signal. Its structure was later adapted for the three-phase case in order to detect the positive-sequence vector of three-phase signals, obtaining the 3phEPLL that is represented in Fig. 5. In this case, each phase voltage is processed independently by an EPLL.

IV. DISCRETE IMPLEMENTATION

The performance of the different structures under test is really dependent on their final digital implementation, particularly on

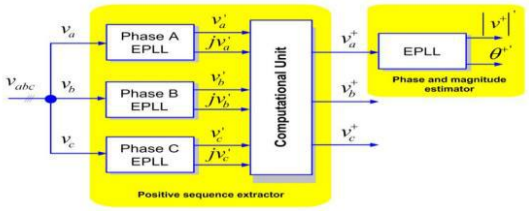

Fig.5.3phEPLL block diagram.

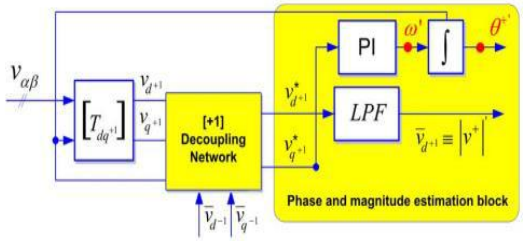

Fig.6. Phase and magnitude estimation loop of the DDSRF PLL.

The discretization approach made to their continuous equations. This implementation is critical and should be studied in detail as a straight forward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL.

In order to facilitate the comprehension of the process, the different building blocks that appear at Figs.3–5 will be referenced. The values of the different parameters used in each case are summarized in the Appendix

A. DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained since the continuous representation

of several parts does not change in the discrete domain. This is the case for the transformation blocks Tαβ, Tdq+1, and Tdq−1 , whose description can be found in general scope literature .

1) Positive and Negative-Sequence Decoupling Networks: The decoupling network constitutes one of the most important contributions of this synchronization method.

2) Phase and Magnitude Estimator Discretization: In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 6).

$$\begin{bmatrix} v^*_{d+1}[n+1] \\ v^*_{q+1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -cos(2\theta'[n]) & -sin(2\theta'[n]) \\ sin(2\theta'[n]) & -cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d-1[n]} \\ \bar{v}_{q-1[n]} \end{bmatrix} \times \begin{bmatrix} v^*_{d-1[n+1]} \\ v^*_{q-1[n+1]} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d-1}[n+1] \\ v_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -cos(-2\theta'[n]) & -sin(-2\theta'[n]) \\ sin(-2\theta'[n]) & -cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d+1[n]} \\ \bar{v}_{q+1[n]} \end{bmatrix} \quad (1)$$

The discrete controller and the integrator can be built using a backward numerical approximation. The frequency and phase can then be represented in the z-domain (2), considering v∗q+1 as the error to be minimized. In this equation, a feed forward of the nominal frequency is given by means of wff

$$W'(z) = \frac{(k_p + k_i.T_s)z - k_p}{z-1}.V^*_{q+1}(z) + \omega ff\theta^{+'} = \frac{T_s.z}{z-1}.W'(z) \quad (2)$$

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p.v^*_{q+1}[n] + (k_p + k_i.T_s).V^*_{q+1}(n+1)\theta^{+'}[n+1] = \theta^{+'}[n] + T_s.\omega'[n+1] \quad (3)$$

In these equations, a frequency feed forward has been introduced as an initial condition to ω.

3) LPF Block Discretization:

The amplitudes of the dq positive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse responses (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency ωf, equal to half of the grid frequency, was originally proposed; hence, the same transfer function has been implemented in this paper for evaluation purposes in

$$y[n] = \frac{1}{T_s\omega_f+1}.x[n] + \frac{T_s\omega_f}{T_s\omega_f+1}.u[n].x[n+1] = y[n] \quad (4)$$

B. DSOGI-PLL Discretization:

1) DSOGI-QSG Block Discretization:

As was previously mentioned in Section II, the DSOGI-based quadrature signal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). In Fig. 7, the block diagram of the implemented SOGI is shown

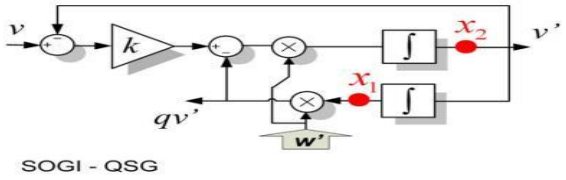

Fig.7. Quadrature signal generator based on a second order generalized integrator (SOGI QSG)

This quadrature signal generator (QSG) is a linear system itself; therefore, a discrete representation can be systematically obtained if the continuous state space is previously deducted. The equations of the SOGI state space appear detailed in (5). Where v constitutes the input while v and qv are the two inquadrature output signals

$$\left.\begin{matrix} \dot{x}_n = A.x_n + B.v \\ y_n = C.x_n \end{matrix}\right\}; \; x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \; y_n = \begin{bmatrix} y' \\ qv' \end{bmatrix}$$
$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k.\omega' \end{bmatrix} \; B = \begin{bmatrix} 0 \\ k.\omega' \end{bmatrix} \; C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix} \quad (5)$$

In these matrices, Ts is the sampling time of the discrete system, ω[n] is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and k is the SOGI gain

$$X[n+1] = A'.x[n] + B'.v[n]$$
$$y[n] = c'.x[n] + D'.v[n] \quad (6)$$

Where Ts is the sampling time.

2) SRF PLL Discretization:

The frequency and phase detection is obtained by means of the SRF PLL shown in Fig. 8.

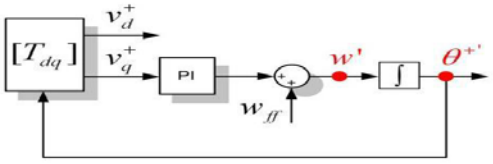

Fig. 8. State variables of the SRF-PLL block.

The discretization of the controller and the integrator is performed using the backward numerical approximation.

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$$W'(z) = \frac{(k_p + k_i.T_s)z - k_p}{z-1}.V^*_{q+1}(z) + \omega ff\theta^{+'} = \frac{T_s.z}{z-1}.W'(z) \quad (7)$$

C. 3phEPLL Discretization

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phase voltages. Discretization: The block diagram of the EPLL implemented in this paper is presented in Fig. 9.

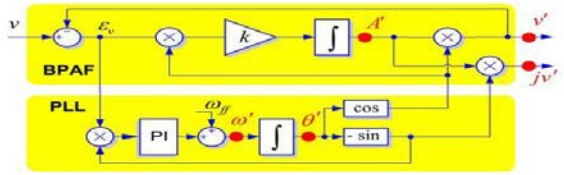


Fig.9. Quadrature signal generator based on an EPLL structure.

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$\dot{A}'(t) = k.e(t).\cos\theta'(t)$$
$$\theta(t) = \omega'(t) + \frac{k_p}{k_i}.\dot{\omega}'(t) \quad (8)$$

Finally, after the state variables are calculated, the EPLL output can be obtained by generating the two quadrature signal

$$V'[n+1] = A'[n+1].\cos(\theta'[n+1])$$
$$qv'[n+1] = -A'[n+1].\sin(\theta'[n+1]) \quad (9)$$

This type of discretization method needs a more accurate tuning, due to the fact that the stable regions of the s-plane and z-plane are different.

2)**Computational Block Unit**: The description for this block is the same in both discrete and continuous domains. Nevertheless, specific equations are used in this paper.

3)**Phase and Magnitude Detection Block:** This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the positive-sequence fundamental component.

V. TESTING S IGNALS AND SIMULATION SETUP

Voltage sags:

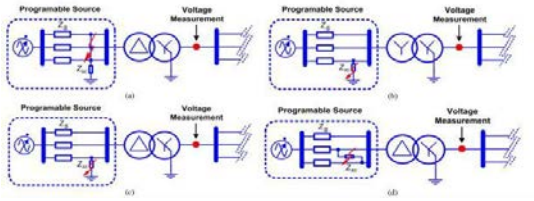
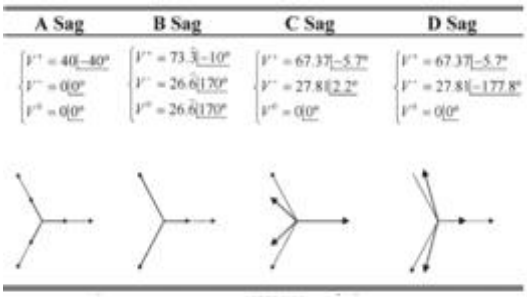


Fig. 10. Generation of grid voltage sags in the experimental setup. (a) Generation of a Type "A" voltage sag. (b) Generation of a Type "B" voltage sag. (c) Generation of a Type "C" voltage sag. (d)
Generation of Type "D" voltage sag.

That these sags are the most characteristic ones that affect wind power systems. In Table I, the magnitude and the phase of the symmetrical components of the voltage during the fault period are indicated in each case, assuming that the pre fault voltage is always equal to V + = 100, V− = 0, and V 0 = 0.

Table I
Properties Of The Testing Voltage Sags



In order to obtain the aforementioned dips, different faults have been emulated with the programmable ac source at the primary winding of the transformer, as indicated in Fig. 11.

• Harmonic-polluted voltage (8% THD):

According to the EN50160 standard, the THD of the voltage waveforms at the output of a generation facility cannot be higher than 8%. Considering this requirement, Table II shows the harmonic composition used for evaluating the performance of the grid synchronization systems under test when the grid voltages become distorted

• Grid voltage frequency jumps:

By means of the programmable source, a 10-Hz jump (from 50 to 60 Hz) in the frequency value of the positive sequence has been applied to analyze the response of the frequency adaptive structures under test.

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Table II
Harmonic Composition for The Test

Order of the harmonic	THD (%)
2^{nd}	2%
4^{th}	1%
5^{th}	5%
7^{th}	4%
11^{th}	3%
13^{th}	3%

VI FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

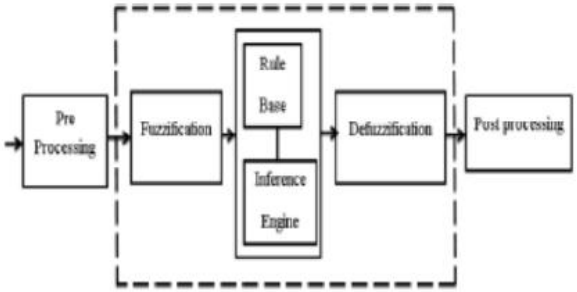

Fig.11.Fuzzy logic controller

Fuzzification: The Partition of fuzzy subsets and the shape of membership CE (k) E (k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

TABLE III: Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph}(k) - P_{ph}(k-1)}{V_{ph}(k) - V(k-1)} \quad (10)$$

$$CE(k) = E(k) - E(k-1) \quad (11)$$

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

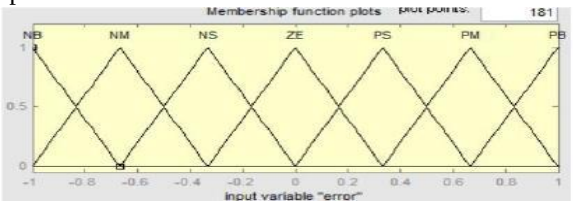

Fig.12.Membership functions

Defuzzification: As a plant usually requires a nonfuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u = -[\alpha E + (1-\alpha)^* c]$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable. A large value of error E indicates that given system is not in the balanced state.

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VII. SIMULATION PERFORMANCE OF THE PLLS UNDER TEST

Behavior of PLLs in Case of Voltage Sags

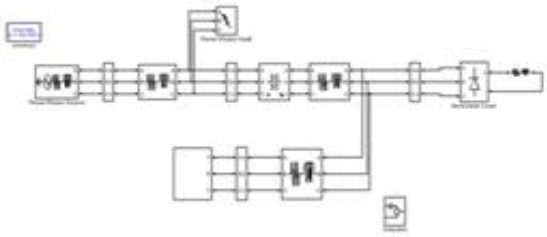


Fig.6.1 General Distribution system

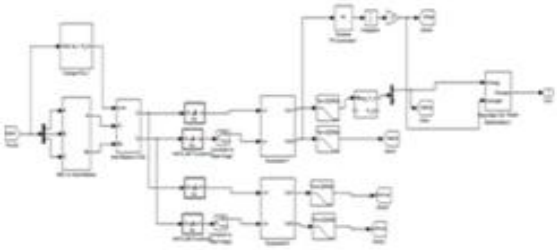


Fig.13 DDSRF PLL

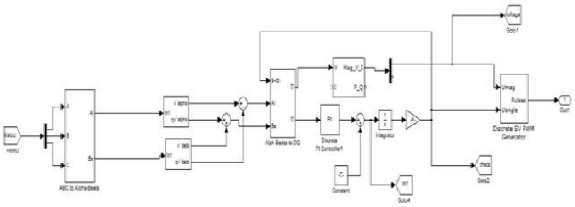


Fig.14 DSOGI PLL

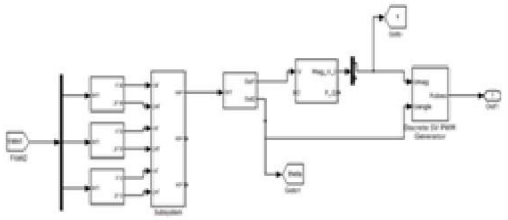
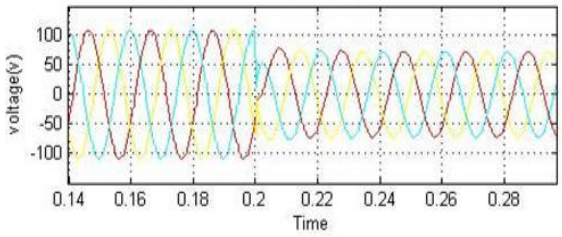
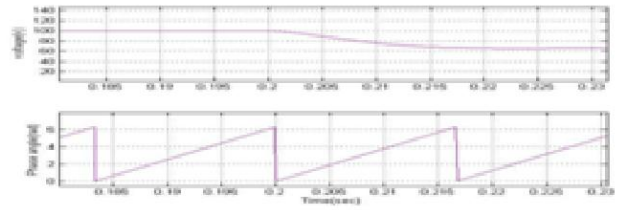


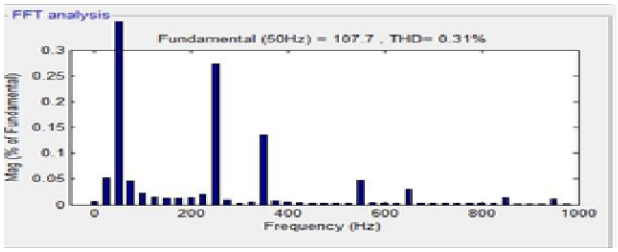
Fig.15 Three phase EPLL

Type A Sag:

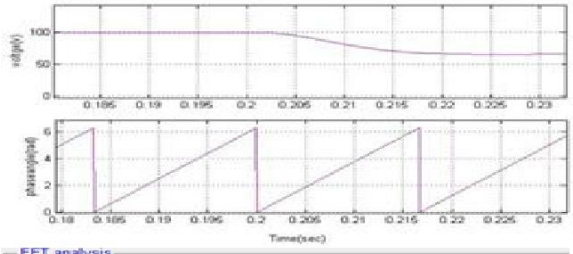


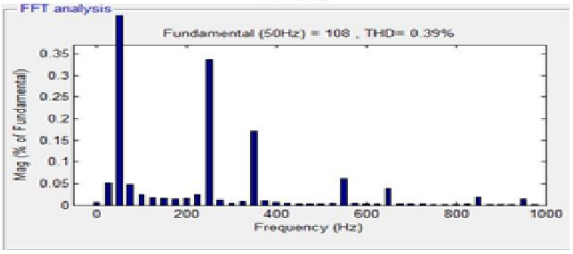
(a) input signal(v)



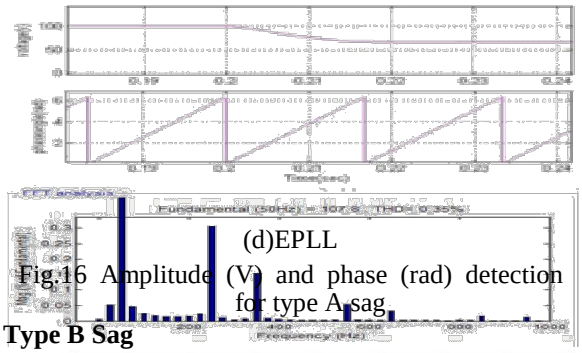


(b) DDSRF PLL





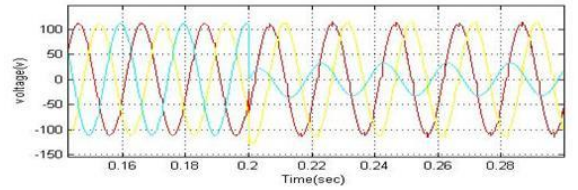
(c)DSOGI PLL



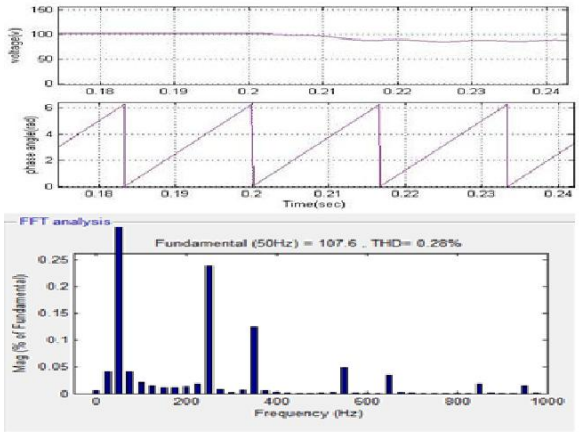
(d)EPLL

Fig.16 Amplitude (V) and phase (rad) detection for type A sag

Type B Sag

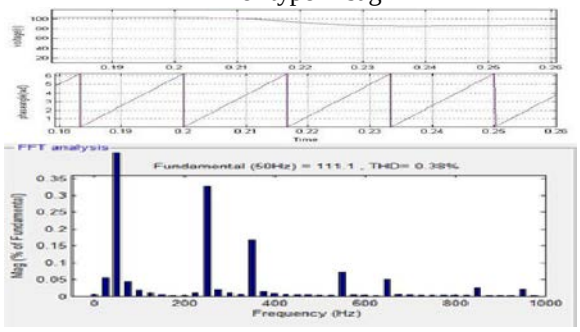


(a) input signal(v)

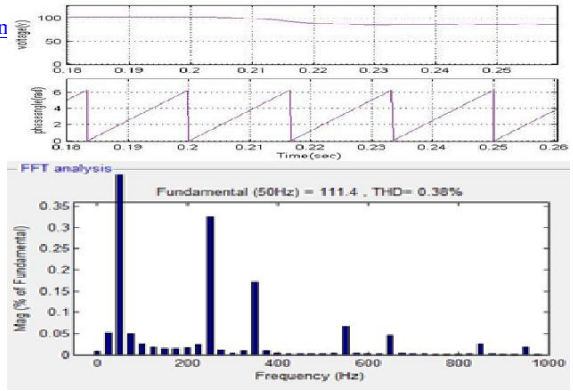


(b) DDSRF PLL

Fig.17 Amplitude (V) and phase (rad) detection for type B sag



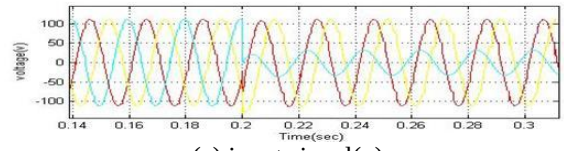
(c) DSOGI PLL



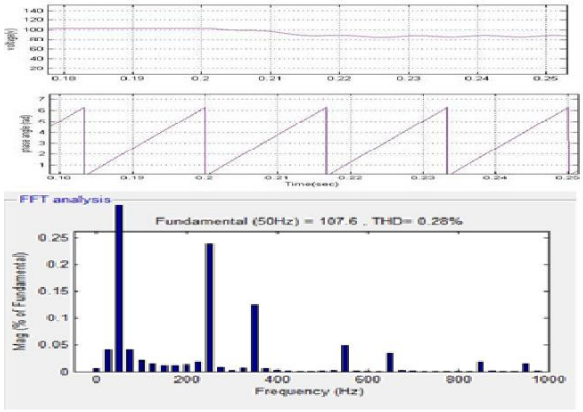
(d) EPLL

Fig.18 Amplitude (V) and phase (rad) detection for type B sag

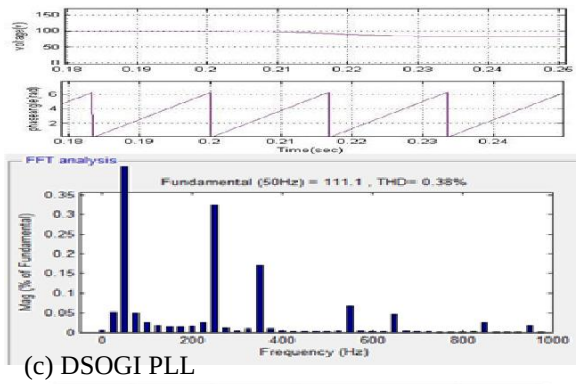
Type C Sag



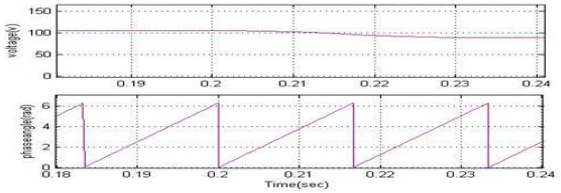
(a) input signal(v)



(b) DDSRF PLL



(c) DSOGI PLL



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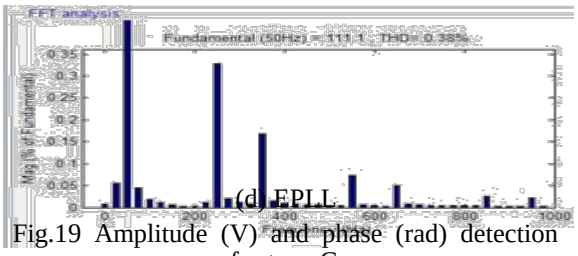
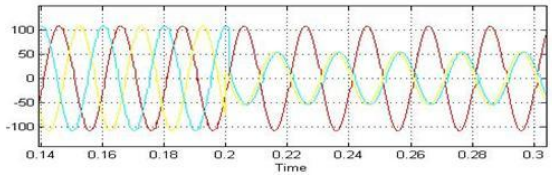


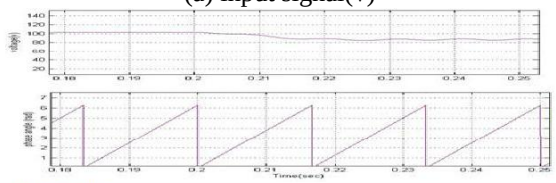
(d) EPLL

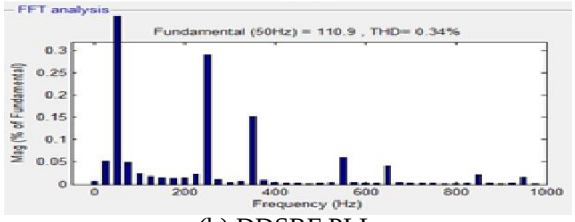
Fig.19 Amplitude (V) and phase (rad) detection for type C sag

Type D sag

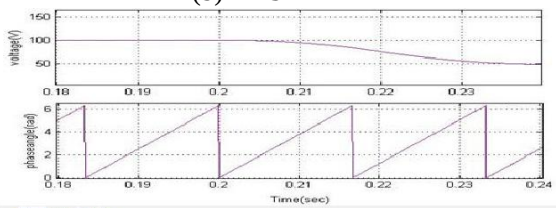


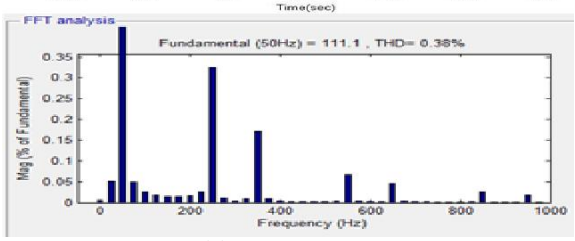
(a) input signal(v)



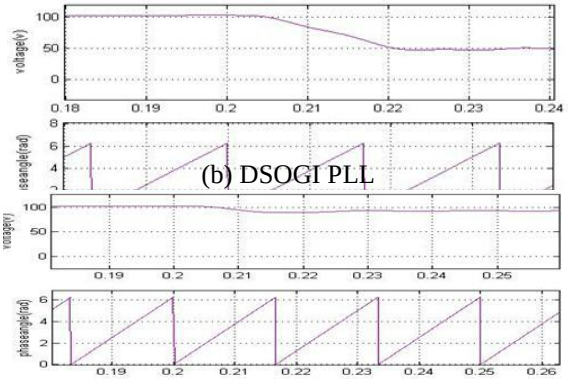


(b) DDSRF PLL

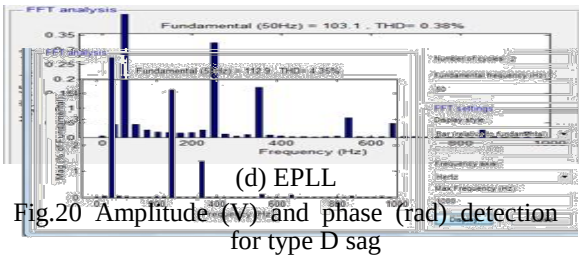




(c) DSOGI PLL



(b) DSOGI PLL



(d) EPLL

Fig.20 Amplitude (V) and phase (rad) detection for type D sag

Behavior of PLLs in Case of Frequency Changes (50–60 Hz)

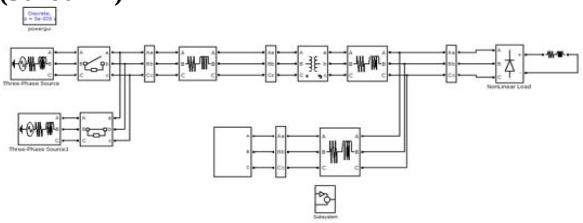
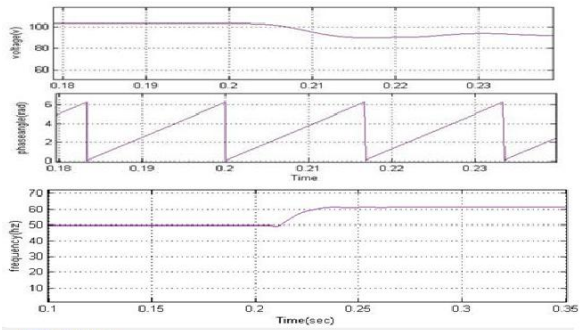
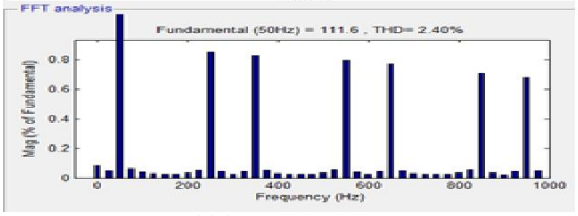
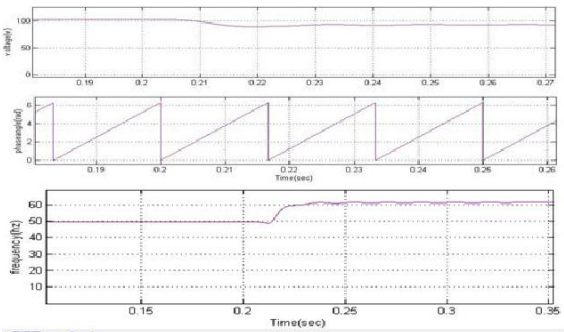


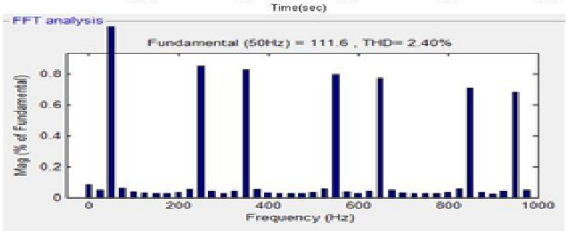
Fig.21 General Distribution system when Frequency changes





(a)) DDSRF PLL





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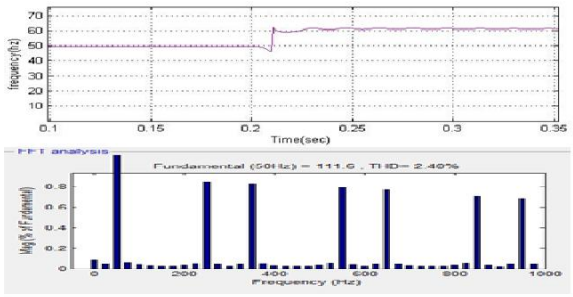


(c) EPLL

Fig. 22 Amplitude, phase, and frequency estimation for frequency changes

Behavior of PLLs in Case of Polluted Grid

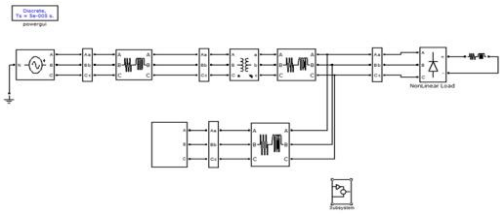
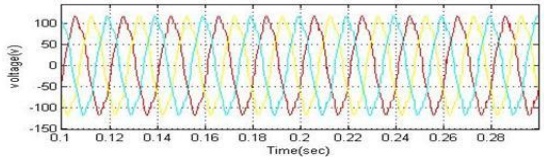
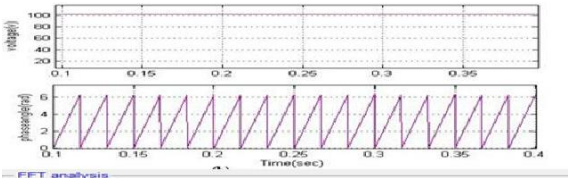


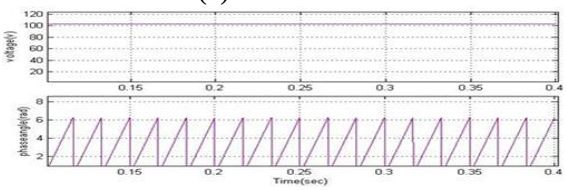
Fig.23 General Distribution system when polluted grid



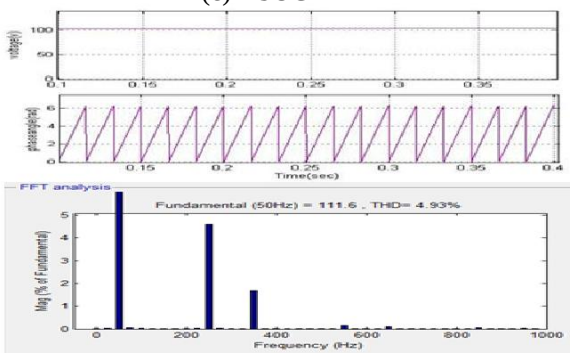
(a) input signal(v)



(b) DDSRF PLL



(c) DSOGI PLL



(c) EPLL

Fig.24 Amplitude (V) and phase detection (rad) for Polluted grid.

Table IV

Number of Operations Performed By Each Pll

Structure	A	M	T	S	D
DDSRF-PLL	22	32	12	14	0
DSOGI-PLL	38	86	4	8	2
3phEPLL-PLL	42	41	19	16	0

VIII. CONCLUSION

This project studied the behavior of three advanced grid synchronization systems by using fuzzy logic controller. Their structures have been presented, and their discrete algorithms have been detailed. The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater band pass and low-pass filtering capabilities. Here we are using fuzzy logic controller instead of using other controllers. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmonics. Although all three have been shown to be appropriate for synchronizing with the network voltage in distributed power generation applications, mainly PV and wind power, the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better tradeoff between the presented systems, making them particularly suitable for wind power applications. The simulation was done by using Fuzzy logic controller.

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