Simulation of Hybrid 9-level Inverter with Reduced Number of Switching Devices for Grid connected load

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Abstract

This paper proposes simulation of a hybrid 9-level inverter using reduced number of switching devices. It can feed maximum power of input PV array to the connected grid with high quality output current with THD of only 0.44%. The level shifted modulation technique is used for the proposed 9-level inverter to generate switching pulses. The conventional multilevel inverter (MLI) has very complicated inverter control, more expensive and difficult to control and regulate the capacitor voltages. Absolute aim of this project is to reduce the number of switches required. The topology consists of two input capacitors and only one auxiliary capacitor. The less number of power components decreases the size of the inverter, weight, circuit complexity and also reduces the cost. Another advantage of this topology is that it increases the efficiency of the system and decreases the switching losses. The simulation is done in MATLAB/SIMULINK R2011b for 1000W system for grid connected load and THD is also obtained.

Keywords: *Multilevel inverter(MLI), Multilevel converter(MLC), Neutral point clamped (NPC), Flying capacitor(FC), Hybrid 9-level inverter, Pulse width modulation(PWM), Maximum Power Point Tracker (MPPT), Total Harmonic Distortion(THD).*

1. Introduction

The multi-level inverter was first introduced in 1975. The three level converters was the first multi-level inverter introduced. A multi-level inverter is a static power electronics circuit that synthesizes stepped form of output voltage from several levels of input DC voltages. With an increasing number of levels in output voltage of an inverter, output waveform approaches to sinusoidal waveform. Renewable energy sources (RES) gain an importance in recent decades because they are pollution free, easily erectable, and limitless. Among RES, Photovoltaic systems are mostly used as they are light, clean and easily installable. To meet high voltage and power requirements, engineer's started developing the multilevel inverter concept and now it has been one of the extensively used inverter in the area of power research.

Multilevel converters (MLCs) were invented with the specific aim of overcoming the voltage limit capability of semiconductor devices. These converters offer numerous advantages compared with the two-level (2L) converter counterpart. The features include good power quality, low switching losses, high voltage capability, and low *dV/dt.* These properties and the advancement in semiconductor technology make MLCs attractive for high-power applications [1]. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage [2,3]. In order to bring the switching component stresses back to acceptable values, new topologies of multilevel converters have been emerging, including five-level topologies [4].

The classic multilevel topologies include the neutral point clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB). Diode clamped MLI require large number of clamping diodes as the level increases .In FC MLI, Switching utilization and efficiency are poor and also it requires large number of capacitors as the level increases and cost is also high. Cascaded H-bridge are mostly preferred for high power applications as the regulation of the DC bus is simple. But it requires separate dc sources and also the complexity of the structure increases as the level predominantly increase. In all these cases the basic target was to generate high quality power output with minimum number of power devices and easier control. The drawback of the 5-level Active Neutral Point Clamped(5L-ANPC) is that the switch voltage ratings are different in different converter branches [5].

The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution [6]. A new coupled inductor based 9-level inverter has only 10 power switches, 4 power diodes and one high frequency coupled inductor to generate nine voltage levels. It improves system efficiency and reduces the size of the system [7]. The use of a coupled split-wound inductor has been described to allow interleaved PWM switching of the upper and lower switches in an inverter leg. The switch control dead times can be eliminated, helping to improve the quality of the PWM voltage generation and increasing the maximum potential output voltage and switching frequency [8]. The transformer-less topologies reduce power losses and cost, the principal problem of such topologies is caused by the parasitic capacitance between ground and PV cell [9]. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10kW [10]. The Renewable sources include solar, wind, biomass, hydro,etc . One of the sources are interfaced into the power production which produces increased reliability, security, flexibility, low power losses and increased power quality [11].

IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 4 Issue 5, May 2017
ISSN (Online) 2348 – 7968 | Impact Factor (2016) – 5.264
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This paper deals with how higher level of output voltage is achieved for a new hybrid 9-level inverter topology using level shifted modulation technique. This topology has the advantages of its reduced number of switching devices, two input dc capacitors and only one flying capacitors compared to the conventional inverter topology for the same levels. The modes of operations are outlined for nine level Hybrid inverter. Simulation of proposed inverter topology is carried out in MATLAB/SIMULINK software.

2. Proposed hybrid 9-level inverter topology

This topology uses a two stage power conversion process as shown in Fig. 1. DC-DC converter is used to boost the low voltage input PV source and as well as MPPT of PV source. Then with the use of MLI nice quality of power can fed in to the load or grid. The proposed topology has 10 power switches, one auxiliary capacitor and one coupled inductor as shown in Fig. 2. There is only one dc source which is split into two with the help of two dc link capacitors (C_1, C_2) to avail clamped neutral point n. Auxiliary capacitor having a voltage equal to one fourth of the dc link voltage, which is used to split the 3-level neutral clamped voltage into 5-levels.9 different voltage levels which can be produced by the inverter are $\pm 4V_{PV}/8$, $\pm 3V_{PV}/8$, $\pm 2V_{PV}/8$, $\pm V_{PV}/8$ and zero as shown in Fig. 3.

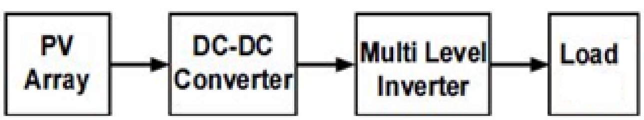

Fig. 1. System block diagram

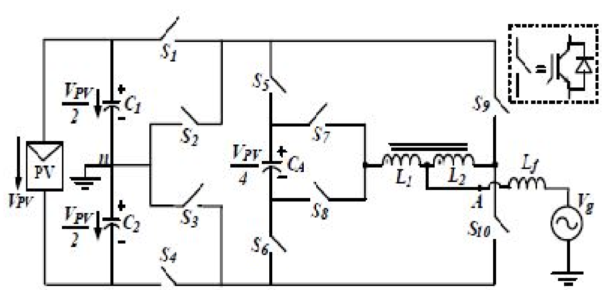

Fig. 2. Proposed hybrid 9-level inverter topology

2.1 States of operations

There are 16 different switching states, which can be used to generate 9 output voltage levels as shown in Table 1. Complimentary switching states can be used to balance the auxiliary capacitor voltage and to control the current through the inductor. Switches S_1 and S_2 are complimentary to each other. Switches S_1, S_3 are turned ON continuously during positive half cycle and switches S_2, S_4 are turned ON continuously during negative half cycle. Similarly switches S_5-S_6, S_7-S_8 and S_9-S_{10} are complimentary to each other. The circuit operates in accordance with switching pattern given in Table 1.

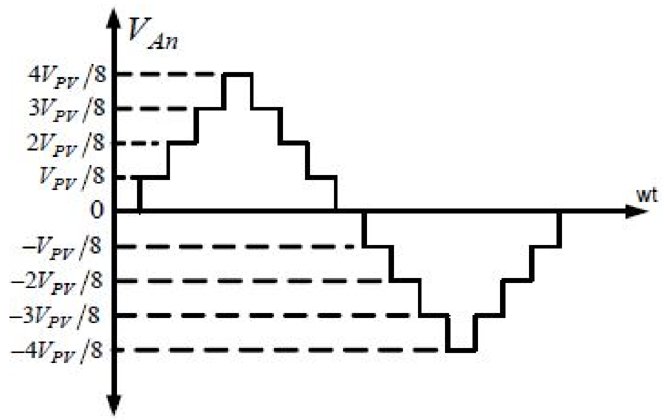

Fig. 3. Proposed topology output voltage waveform

Table 1: Switching pattern for hybrid 9-levelinverter

States	Switching State										V_{An}
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	
1	1	0	1	0	1	0	1	0	1	0	$4V_{PV}/8$
2	1	0	1	0	1	0	0	1	1	0	$3V_{PV}/8$
3	1	0	1	0	0	1	1	0	1	0	$3V_{PV}/8$
4	1	0	1	0	0	1	0	1	1	0	$2V_{PV}/8$
5	1	0	1	0	1	0	1	0	0	1	$2V_{PV}/8$
6	1	0	1	0	1	0	0	1	0	1	$V_{PV}/8$
7	1	0	1	0	0	1	1	0	0	1	$V_{PV}/8$
8	1	0	1	0	0	1	0	1	0	1	0
9	0	1	0	1	1	0	1	0	1	0	0
10	0	1	0	1	1	0	0	1	1	0	$-V_{PV}/8$
11	0	1	0	1	0	1	1	0	1	0	$-V_{PV}/8$
12	0	1	0	1	0	1	0	1	1	0	$-2V_{PV}/8$
13	0	1	0	1	1	0	1	0	0	1	$-2V_{PV}/8$
14	0	1	0	1	1	0	0	1	0	1	$-3V_{PV}/8$
15	0	1	0	1	0	1	1	0	0	1	$-3V_{PV}/8$
16	0	1	0	1	0	1	0	1	0	1	$-4V_{PV}/8$

1) *MODE-1*:
In this mode power switches S1, S3, S5, S7 and S9 are turned on simultaneously and the complimentary switches are kept in OFF condition. The output voltage across V_{An} is $4V_{PV}/8$.

2) *MODE-2:*
In this mode power switches S5, S8, and S9 are turned on at a time. The output voltage across V_{An} is $3V_{PV}/8$.

3) *MODE-3:*
This mode is complimentary to that of mode 2 .Switches S6, S7, and S9 are turned ON simultaneously. The corresponding output voltage across V_{An} is $3V_{PV}/8$.

4) *MODE-4:*
In this mode power switches S6, S8, and S9 are turned on simultaneously. The output voltage across V_{An} is $2V_{PV}/8$.

5) *MODE-5:*
This mode is complimentary to that of mode 4. Switches S5, S7, and S10 are turned ON simultaneously. The corresponding output voltage across V_{An} is $2V_{PV}/8$.

6) *MODE-6:*
In this mode power switches S5, S8, and S10 are turned ON simultaneously. The output voltage across V_{An} is $V_{PV}/8$.

7) *MODE-7:*
This mode is complimentary to that of mode 6 .Switches S6, S7, and S10 are turned ON simultaneously. The corresponding output voltage across V_{An} is $V_{PV}/8$.

8) *MODE-8:*
In this mode power switches S6, S8, and S10 are turned ON simultaneously. It generates an output voltage of zero in positive half cycle. Similarly Mode 9 generates output voltage of zero in negative half cycle.

The switching pattern as discussed in Mode 1 to Mode 8 can be used to generate positive output voltage levels. Similarly Mode 9 to Mode 16 can be used to generate negative output voltage levels.

3. PWM techniques and control strategy

3.1 PWM technique

The level shifted modulation technique is used for the proposed hybrid 9-level inverter to produce switching pulses. Single modulating wave V_m is used to compare with four different carrier waves CR1, CR2, CR3 and CR4 to generate switching pulses in the positive half cycle. Similarly same modulating wave V_m is used to compare with four different carrier waves CR1-,CR2-,CR3-, and CR4- to generate switching pulses in negative half cycle as shown in Fig. 4.

3.2 Control strategy

The main focus of the implemented control strategy is to extract maximum power from the PV source and fed it to the grid connected load. The control strategy for the proposed inverter is shown in Fig. 5.

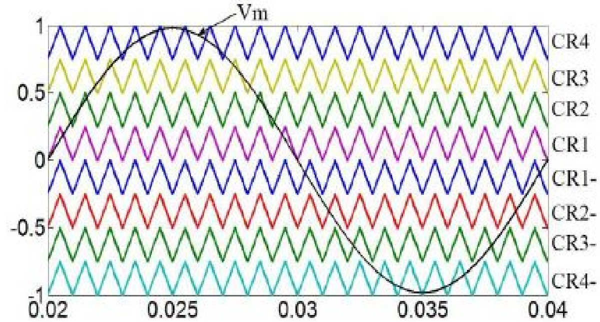

Fig. 4. PWM technique for the proposed 9-level inverter

The control strategy operates in three different steps:

- The MPP voltage and currents computation.
- Deciding the modulating signal phase and amplitude
- Switching pulses generation.

PI controller is a combination of Proportional and Integral controllers. The forced oscillation and steady state error will be eliminated by this and they are most commonly used in industries. Tuning of the PI controller is a very important task. Fine tuning is necessary to obtain appropriate output. The overall simplicity and efficiency of the PV system depends on the MPPT technique employed.

PV voltage and current are sensed and the MPP voltage (V_{mpp}) and currents (I_{mpp}) are calculated through a Purturb & Observe algorithm in order to extract maximum power from the solar PV module. The reference voltage V_{mpp} is compared with the actual voltage of PV module V_{PV} to generate error signal(e_m). This error e_m is fed to the PI controller, then required peak of the load current (i_d^*) is obtained. The obtained i_d^* is used to calculate the reference current for the second step (for generating modulating signal). In the second step, the PLL output is multiplied with peak of the load current(i_d^*) in order to calculate reference current (i_g^*). By comparing the reference current (i_g^*) and the load current (i_g) the error signal (e_c) is generated. This error signal is passed through the PR controller to generate the modulating signal (m_a). At last, the desired switching pulses is generated by using the resulting modulating signal.

IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 4 Issue 5, May 2017
ISSN (Online) 2348 – 7968 | Impact Factor (2016) – 5.264
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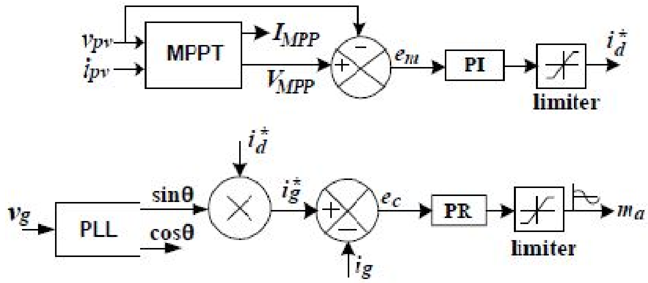

Fig. 5. Control strategy for the proposed 9-level inverter

The values of PI controller are K_P=0.1 and K_i=10. The load Current is controlled by using PR controller. The obtained PR controller is given by $s^2+314.1s+98596/s^2+157s+98596$.

4. Comparison of different topologies

The 9-level active ANPC MLI [4] uses more number of switches and auxiliary capacitors. The Nested Neutral Point clamped(NNPC) converter for medium voltage power conversion [5] and the hybrid ANPC FC MLI uses even more number of auxiliary capacitors than the ANPC MLI [4]. Coupled inductors based MLI [7,8] consists of less number of devices. The proposed topology uses minimum number of power switches in comparison to other 9-level inverters as shown in Table 2.

Table 2: Proposed inverter compared to other existing 9-level inverters

	FC	NPC	Cascaded H-Bridge	MMC	FC-ANPC	Proposed
DC Source	1	1	4	1	1	1
Input capacitors	8	8	4	0	2	2
Auxiliary Capacitors	7	0	0	16	3	1
Auxiliary Diodes	0	14	0	0	0	0
Power switches	16	16	16	32	12	10
Coupled inductor	0	0	0	0	0	1
Loss distribution	Very good	Poor	Good	Good	Fair	Good
Voltage stress across the power switches	$V_{pv}/8$	$V_{pv}/8$	$V_{pv}/4$	$V_{pv}/8$	$V_{pv}/2$	$V_{pv}/2$

5. Simulation results

The analysis of proposed hybrid 9-level inverter is carried out in MATLAB/SIMULINK software. Here MOSFETs are used to work as switches in place of S1 to S10. Scopes are used to measure output voltage, output current and voltage across input and auxiliary capacitors. Table 3 shows model specifications of the proposed hybrid 9-level inverter. The switching pulses and output voltage and output current waveforms for grid connected load as shown in Fig. 7 and Fig. 8 and Fig.9 respectively. The THD also obtained by simulating main circuit in MATLAB. Fig.12 represents the %THD present in the output current waveform of the proposed inverter. Fig.13 represents Voltage and current waveforms of solar PV module at MPP.

Table 3: Model specifications

1	PV source voltage: V_{PV}	400V
2	Power rating of the system	1000W
3	%THD	0.44
4	Input capacitor: C_1, C_2	3300mF
5	Auxiliary Capacitor: C_A	7600e-4
6	Carrier wave frequency	3kHz
7	Self inductances: L_1, L_2	4mH
8	Output voltage	190V

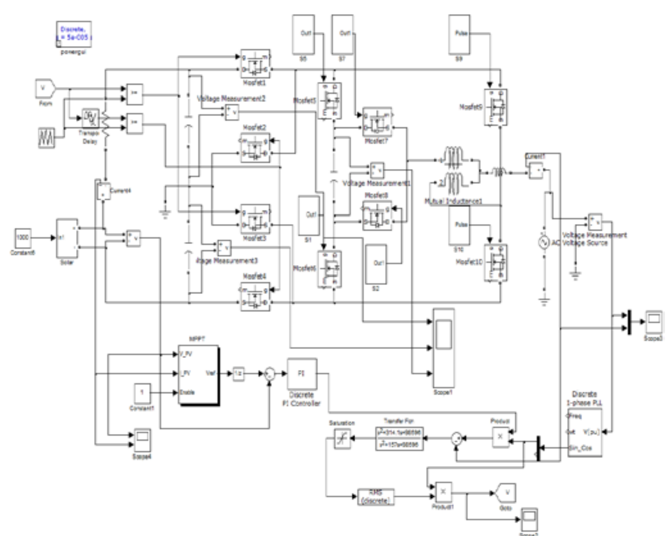

Fig. 6. Simulink model of hybrid 9-level inverter with Grid connected load

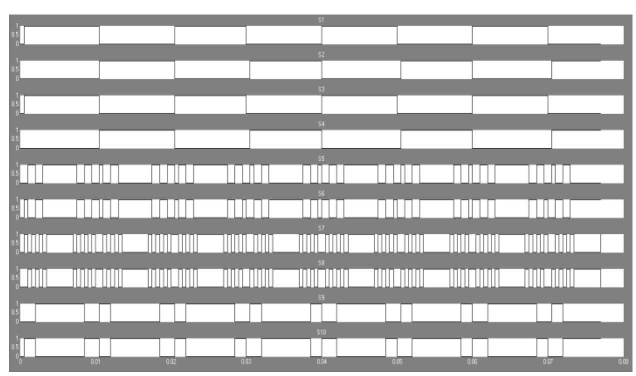

Fig. 7. Switching pattern of switches S1 to S10

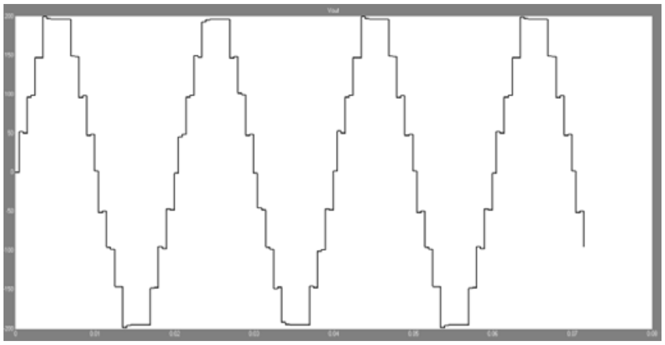

Fig. 8. Output voltage waveform of hybrid 9-level inverter

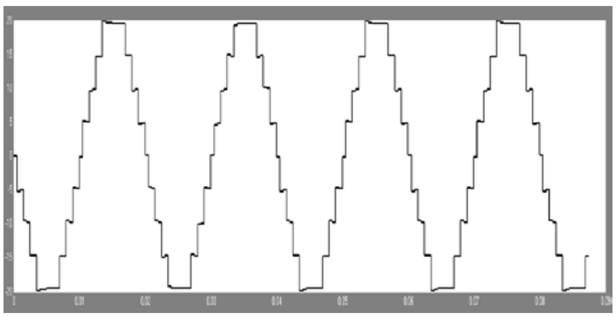

Fig. 9. Output current waveform of hybrid 9-level inverter

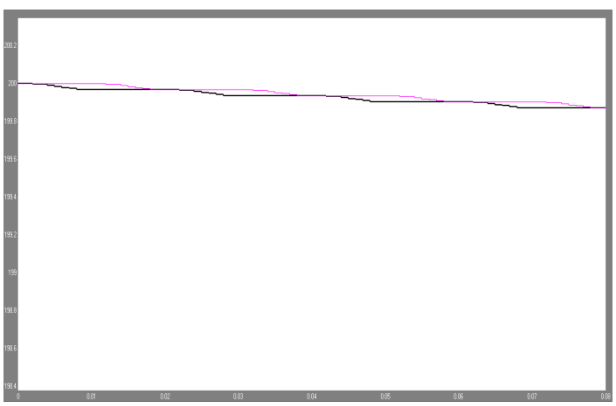

Fig. 10. Input capacitors (C1, C2) voltage waveforms

Fig. 11. Auxiliary capacitor (C_A) voltage waveform

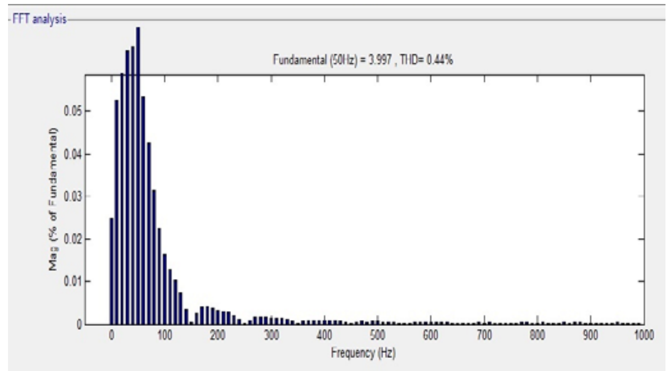

Fig. 12. THD analysis of output current

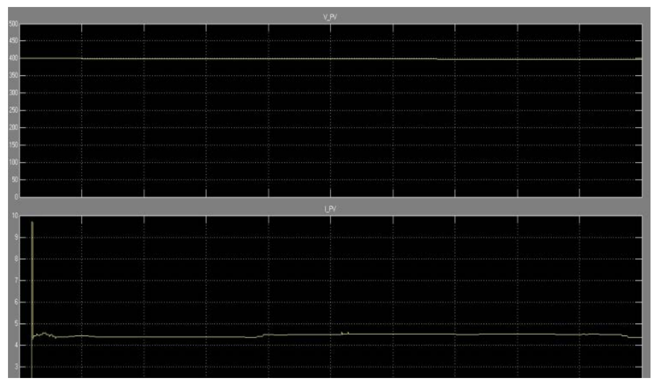

Fig. 13. Voltage and current waveforms of solar PV module at MPP

6. Conclusion

Simulation of hybrid 9-level inverter with grid connected load is carried out in MATLAB Simulink R2011b. The number of switching devices required is very less compared to the other 9-level multi-level inverters. It can feed maximum power of input PV array to the connected load with high quality output current with THD of only 0.44%. As the number of switches is reduced, the overall cost, size, driver circuits required are reduced. So this topology is cost-effective. The less number of power components also results in reduced switching losses, increased reliability and higher efficiency. This topology also provides better loss distribution and better inverter control.

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