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Performance of CMOS and DTMOS Sense Amplifier for SRAM Application for Different Topologies

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Abstract- In this paper comparison between CMOS and DTMOS amplifiers for SRAM application using 180nm and 90nm topology is done. The tool used for simulation is Cadence Tool. The power dissipation varies with variation in supply voltage. The delay and average power dissipated for various values of power supply has been discussed and reported. The DTMOS sense amplifier is preferred at lower supply voltages for high speed applications.

Keywords – Power dissipation, delay, SRAM, DTMOS, CMOS, Sense Amplifier

I. INTRODUCTION

In designing of memory cell, sense amplifiers are used to get lesser power dissipation and delay. Depending upon the performance various types of sense amplifiers are used in designing the memory. The delay should be very low so that it can be detected even if there is a small change on the bit lines due to the read and write operation in sense amplifier. [1]
The various designs are compared based on delay and power consumption for different supply voltages. In this paper DTMOS and CMOS circuits are compared which has 3 transistor stages between VDD to GND. For DTMOS, the transistor's gate and substrate are connected together and due to the body effect, the threshold voltage can be changed dynamically in MOSFET. DTMOS is an excellent technique to get lesser delay. [2]

II. CIRCUIT DESCRIPTION AND OPERATION

A. CMOS (Complementary MOSFET) Sense Amplifier

In this circuit, there are 3 transistor stages between VDD to GND, and bitlines B and B' are cut off from the output nodes O and O' as shown in Fig1 and its circuit diagram in Cadence tool is shown in Fig3. When SE =0, the transistors, MP1, MP4, MN5 and MN6 will be enabled, and MP5, MP6 will be disabled. Therefore, the transistors MP5 and MP6 will be isolated from the input signals coming from bit lines. Nodes 1 and 2 are connected to GND by MN5, MN6, so MN3, MN4 will be disconnected. The output nodes will be charged to the VDD by the transistors MP1, MP4. As MN3, MN4 are turned off, both the output nodes will hold the VDD level. [3][4]
When SE=1, the transistors, MP5, MP6 will be enabled and MN5, MN6, MP1, MP4 will be disabled. The bit lines signals from the transistors MP5 and MP6 are given to the gates of transistors MN3 and MN4. The voltage difference between the gates of transistors MN3 and MN4 induces a drain-to-source current difference between them. This current difference will be converted and amplified to a voltage difference between output nodes O and O' by the amplifier which consist of MP2, MP3, MN1 and MN2. The full swing voltage level will be available at the output nodes for a very short period of time. [3][4]

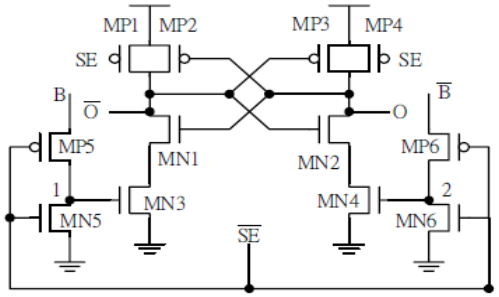

Fig1: CMOS Sense Amplifier

B. DTMOS (Dynamic Threshold Voltage MOSFET) Sense Amplifier

For DTMOS sense amplifier as shown in Fig2 and its circuit diagram in Cadence tool is shown in Fig4, the circuit and working is same as above CMOS sense amplifier. In DTMOS gate and substrate of the transistors are coupled together and due the body effect, the threshold voltage can be changed dynamically in MOSFET during the different modes of operation. When input given to the transistors is low, p-MOS is enabled with low V_{th} and n-MOS is disabled with normal $V_{th.}$ In active mode due to the low V_{th} p-MOS, the circuit get switched from low to high with a higher speed. In the standby mode, the subthreshold current of high V_{th} transistor decides the static leakage current which is smaller. When input to the transistors is 'high', the working is vice-versa. [2]

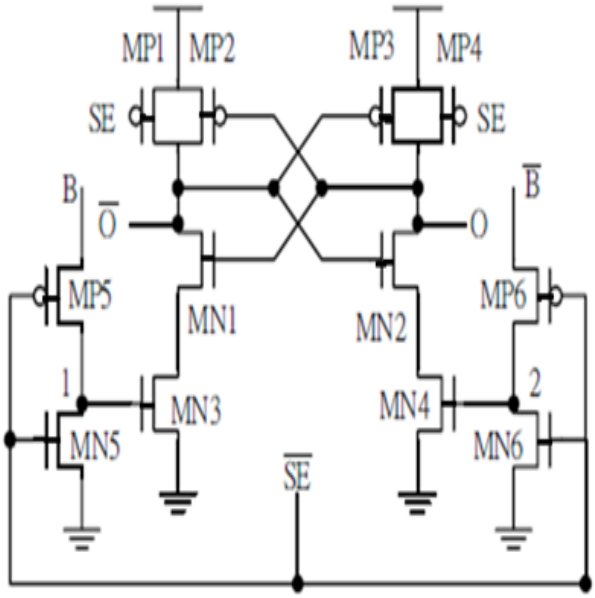

Fig2: DTMOS Sense Amplifier

III. DESIGN AND SIMULATION RESULTS OF SENSE AMPLIFIER

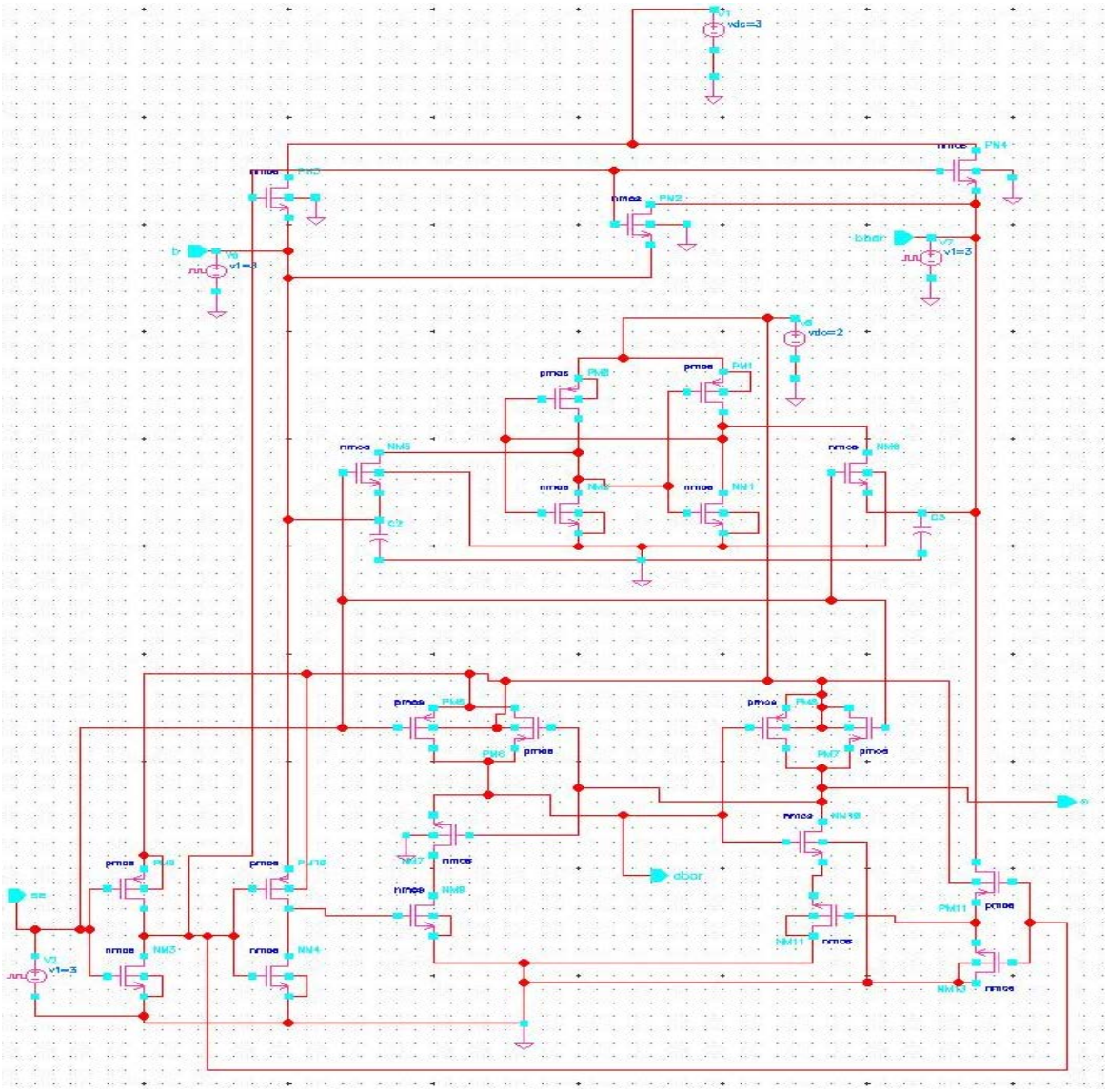

Fig3: Circuit Diagram of CMOS sense amplifier in Cadence Tool

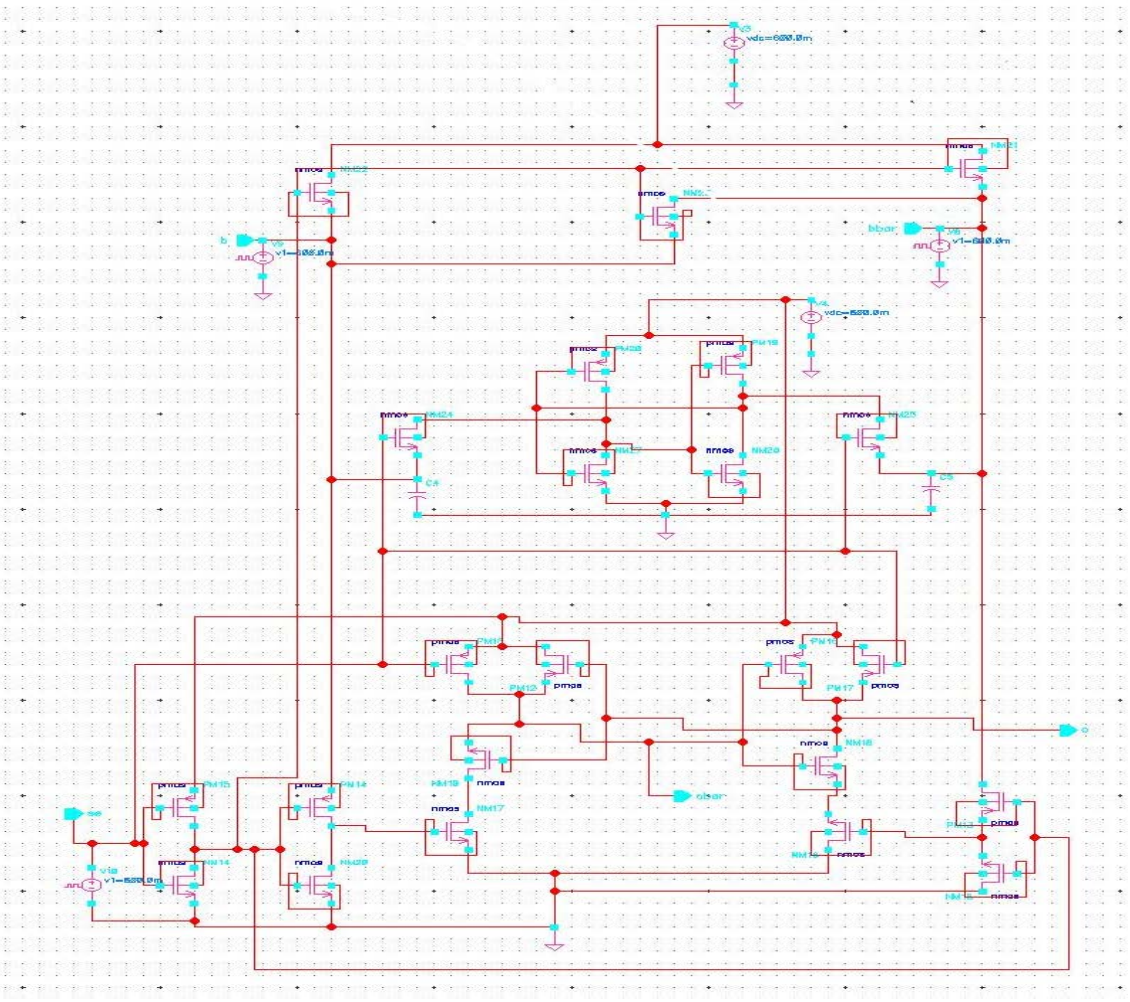

Fig4: Circuit Diagram of DTMOS sense amplifier in Cadence Tool

TABLEI: Variation of Power Consumed and Delay for CMOS and DTMOS Sense amplifiers for 180nm

S.NO.	VDD(V)	CMOS		DTMOS	
		POWER(W)	DELAY(S)	POWER(W)	DELAY(S)
1	0.3	$6.678*10^{-9}$	$225.3*10^{-9}$	$89.57*10^{-9}$	$6.44*10^{-9}$
2	0.4	$4.19*10^{-6}$	$115.8*10^{-9}$	$1.206*10^{-6}$	$40.04*10^{-9}$
3	0.5	$1.613*10^{-6}$	$85.91*10^{-9}$	$13.1*10^{-6}$	$19.74*10^{-9}$
4	0.6	$12.37*10^{-6}$	$27.72*10^{-9}$	$128.8*10^{-6}$	$17.22*10^{-9}$

TABLEII: Variation of Power Consumed and Delay for CMOS and DTMOS Sense amplifiers for 90nm

S.NO.	VDD(V)	CMOS		DTMOS	
		POWER(W)	DELAY(S)	POWER(W)	DELAY(S)
1	0.3	$1464.9*10^{-9}$	$16.43*10^{-9}$	$609*10^{-9}$	$16.4*10^{-9}$
2	0.4	$4.689*10^{-6}$	$15.62*10^{-9}$	$3.174*10^{-6}$	$15.6*10^{-9}$
3	0.5	$7.566*10^{-6}$	$15.46*10^{-9}$	$8.49*10^{-6}$	$15.4*10^{-9}$
4	0.6	$15.39*10^{-6}$	$15.4*10^{-9}$	$28.93*10^{-6}$	$15.3*10^{-9}$

IV. CONCLUSION

In this paper CMOS and DTMOS sense amplifiers are compared based on power dissipation and delay as shown in Table I and II for 180nm and 90nm respectively. The power dissipation decreases with decrease in supply voltage and is minimum at 0.3 volt for both 180nm and 90nm topology. For DTMOS sense amplifier, delay is low for 90nm topology and power dissipation is also low for 90nm topology for 0.4 to 0.6 volts supply voltage. For CMOS sense amplifier, delay is low for 90nm but power dissipation is high for 90nm topology. From the results obtained, DTMOS sense amplifier has lower delay as compared to CMOS sense amplifier for both topologies.

V. REFERENCES

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