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Scheming of 4-bit CMOS Arithmetic Logic Unit using Efficient Logic Techniques

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Abstract

Combinational circuits for mathematical operations are the important components of a processing unit where its throughput is determined and is utilized in the ALU. Here we are focusing on the low-power implementation techniques for several digital circuits for high-performance combinational circuits for mathematical use for optimization based on performance for each watt and to recognize silicon area efficiency. Several methods are being presented and it is found that Dual Value Logic is more efficient in energy consumption which provides better performance. The double-pass transistor logic method is observed with better circuit implementation with less supply where Complementary-pass-transistor logic gives the most remarkable performance with high efficiency. All these three methods are combined together and the adder time as well as subtractor time of a ALU chip is made-up in 180 nm CMOS technology with cadence spectra simulation, it is observed that, the method produced simulation time of 1000ns at a supply voltage of 1.8v.

Key words: *CMOS, ALU, logic circuits etc.*

1. Introduction

Now in these days, demand for less power VLSI with improved performance and efficiency tends to design more effectively by their layout, logic levels, technology and basic architecture of design [4]. When taking into consideration of logic design of combinational logic circuits, one has to look for its less power consumption, more level of achievement, utilization of less space, more speed of operation and mostly with high efficiency. The different parameters affecting the above conditions are any short circuit and leakage current, activities on transition and power dissipation switching capacitance. Now it becomes more vital to choose proper design of circuit and efficient method of implementation by restricting the formulation of universal regulations for optimal logic styles. Investigations of the process are mainly considered on full-adder, full subtractor, and multiplier circuits used in different arithmetic operations. During this work, examination of different process with more set of logic gates for arbitrary combinational circuits is carried out.

2. Complementary CMOS

In complementary CMOS logic design using gates are designed from a pull-down NMOS and a dual pull-up PMOS logic structure. By using both the logic structures, many types of logic functions can be realized and it can be achieved by connecting the output of the gate with the power lines. The major merits of CMOS circuit are it is robust in nature against the transistor space and scaling of voltage with more noise margin. It provides very reliable function at very less voltage with minimum transistor size. The layout of CMOS is simple and efficient for its non-complementary pairs of transistors. The major drawback in CMOS is its high input loads as there is huge number of PMOS transistors are used [8]. Other disadvantage is the weak output driven ability where delay increases due to connection of series of transistors at the output section [9].

2.1 CMOS 4-bit Adder Cell

General CMOS is utilized in almost all digital logic circuits for different application. Beside that other several logic circuits are also used in industries for specific applications. As our focus lies to design a structure which gives low power consumption with better performance in minimal size. Figure-1 shows the basic diagram of a static CMOS full adder cell [1]. The p-channel MOSFET network of every stage is the dual step network of the n-channel MOSFET. The width of the serial n-channel MOSFET or p-channel MOSFET tends to increase for obtaining a conductivity to drive the capacitive loads. For this significant area overhead and high gate input capacitance results for which dissipation of high power

occurs. Due to more input capacitance, rise in delay takes place.

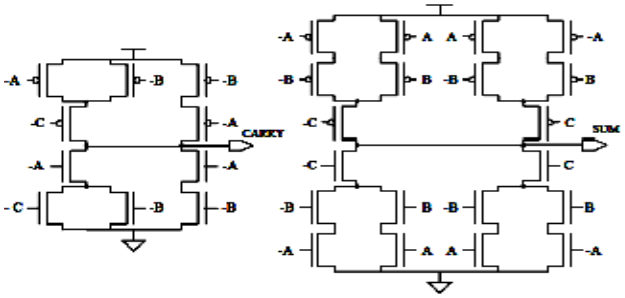

Figure-1: Static CMOS 4-bit Full Adder cell

Figure-2 shows a block diagram of a multiple full adders for addition of N-bit numbers. Output of each full adder is fed to the input of next full adder circuit where first one is the half adder circuit.

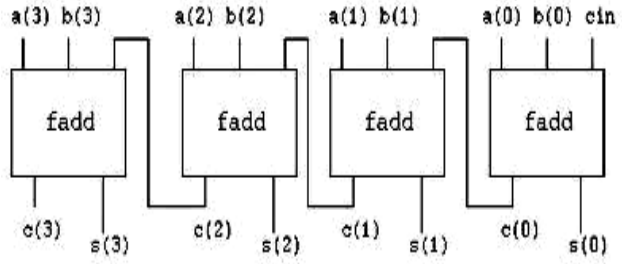

Figure-2: Block diagram of CMOS 4-bit Full Adder Cell

2.2 CMOS 4-bit Subtractor Cell

Figure-3 shows a block diagram of a multiple full subtractors for subtraction operation. Input of each full subtractor is output of previous full subtractor where first one is the half subtractor circuit.

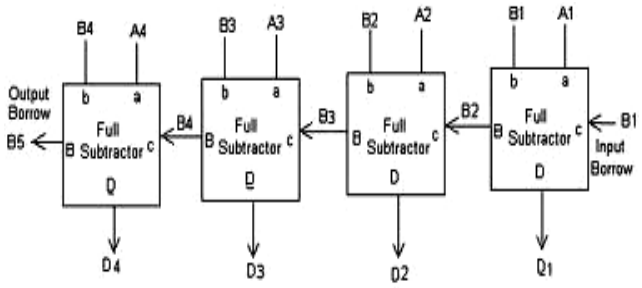

Figure-3: Block diagram of a 4-bit Full Subtractor cell

2.3 CMOS 4-bit Multiplier Cell

General digital binary multiplier is constructed with binary adders. Mostly these methods are involved for computation of a set of partial products after that summing them jointly. This method is used for conducting lengthy multiplication on base-10 integers. Here we modify it for application to binary numbers. Figure-4 shows the structure of a 4X4 binary multiplier cell.

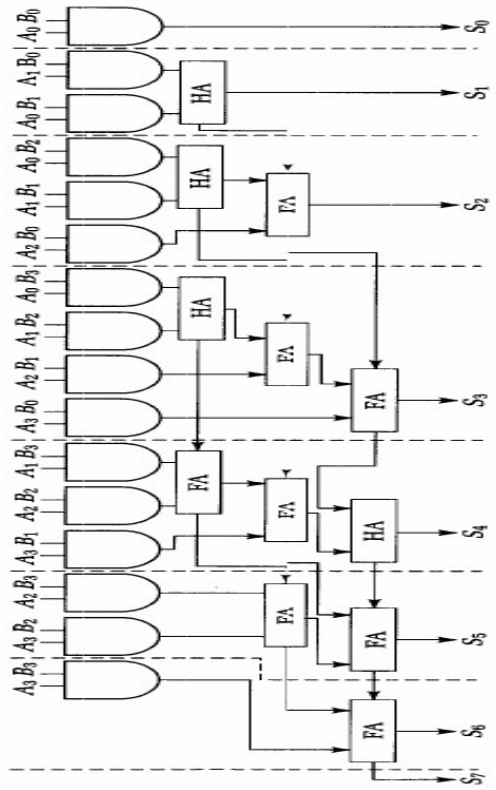

Figure-4: Block diagram of a 4X4 Multiplier cell

3.0 Efficient logic techniques

3.1Complementary Pass-Transistor Logic

CPL design is a combination of complementary inputs/ outputs, NMOS pass-transistor network along with CMOS output inverters. The output signals are restored by CMOS inverters because of the minimal voltage of NMOS transistor drops to pass-transistor's output nodes. For its small input capacitance and less transistor, CPL is useful for the arithmetic building blocks with better speed.

Yano et al. [10] implemented a technique using a network of n-MOSFET type pass-transistors for Boolean functions. During comparison it is found that the full static CPL implementation utilizes only 50% transistors and it avoids the problem on designing in serially connected transistors in pull-up and down planes**.** It was also observed in CPL that, if the outputs of n-MOSFET network are logically high at *Vdd-Vt* then an incomplete turn-off of p-MOSFET is produced in the inverters as results high static current flows. To minimize the current, a fragile p-MOSFET feedback device is connected to the output inverter stage for pulling the output node of the pass-transistor to *Vdd.* But MOSFET's pull-up increases delay of the CPL gate. A low-power consumption CPL may be formed by introducing two CPL gates.

CPL Full Adder Cell

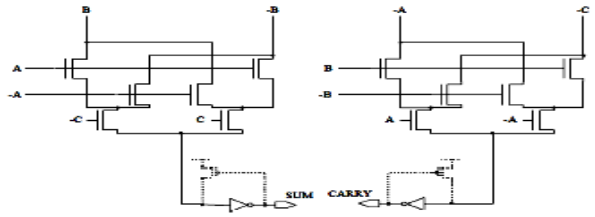

Figure-5: Block diagram of CPL Full Adder cell

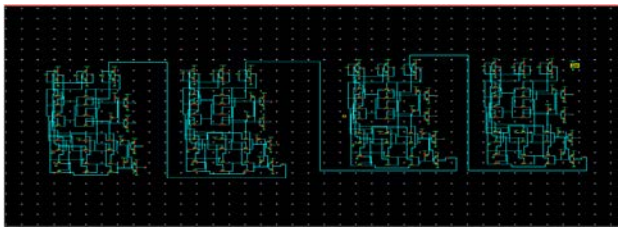

Figure-6: Schematic diagram of a 4-bit CPL Full Adder cell

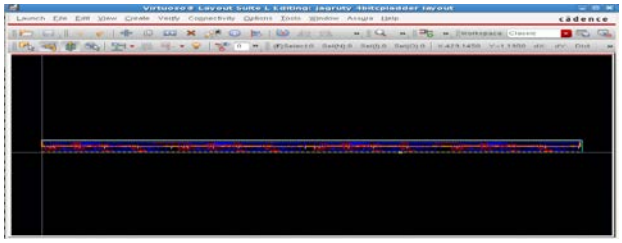

Figure-7: Layout design of a 4-bit CPL Full Adder cell

CPL uses only an n-channel MOSFET structure during the implementation of logic functions for obtaining low input capacitance and high-speed operation [13, 14]. Different diagram related to CPL full adder cell is shown in figure 5,6 and 7. There is a need of a amplification of the signals using CMOS inverters at the output because the high voltage level at the output of pass-transistor is lower than the supply voltage.

CPL Full Subtractor Cell

Different sizes of sub micron feature are taken during the analysis which yielding the gate structure of the design circuit and its corresponding supply voltage. The proposed technique is designed for submicron region where it obtains a less power consumption and dissipation [13, 14]. The proposed technique for subtractor cell is found to be useful for sensing the unwanted as well as wanted signals during signal propagation.

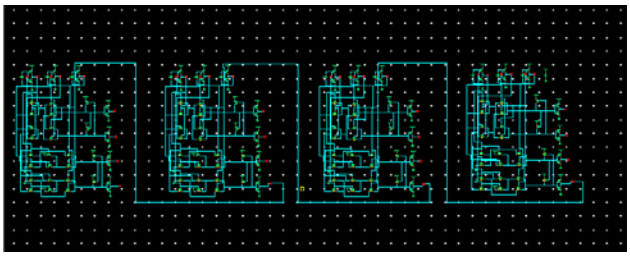

Figure-8: Schematic diagram of a 4-bit CPL Full Subtractor cell

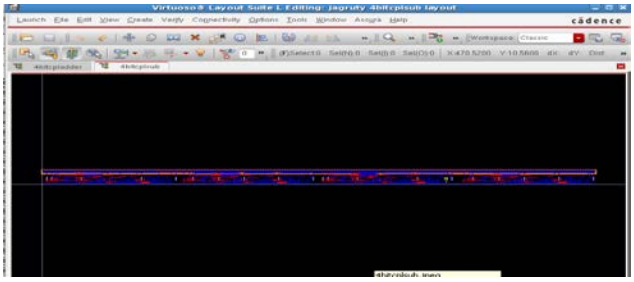

Figure-9: Layout design of a 4-bit CPL Full Subtractor cell

CPL Multiplier Cell

The design of a 4 X 4 binary multiplier cell was designed in this work by utilizing differential CMOS logic family called Complementary Pass-transistor Logic [13, 14]. Here CPL is structured with differential logic without the use of PMOS latching load. Aim is to make the speed twice as fast as traditional CMOS and to make less power dissipation by the use of small input capacitance. By comparing the various speed devices, the multiplier produces much faster at both 77K and 300 K provided that the half- micrometer CMOS technology fully utilizing CPL with lesser power dissipation capability. It is

observed that, by using half-micrometer CMOS with entirely utilizing CPL have a 100-MHz repetition rate of performance potential. Figure-10 shows the schematic of a 4X4 CPL multiplier cell.

As we use slightly additional number of transistors in the design circuit, there is a extra bit of power dissipation in the proposed CPL multiplier cell. As compared to other multipliers, stabilization in performance of the CMOS multiplier cell is carried out by reducing the supplied voltage. It is found to be the proposed CPL multiplier cell is producing better performance at low voltages.

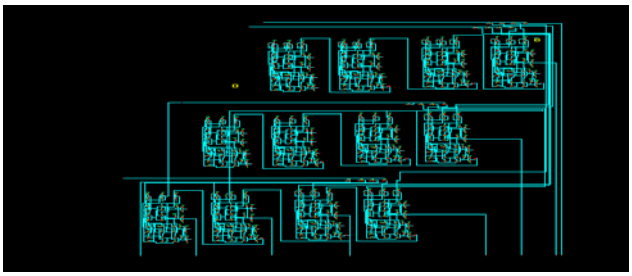

Figure-10: Schematic diagram of a 4X4 CPL Multiplier cell

3.2 Double Pass-Transistor Logic

Double pass transistor logic [2] utilizes both NMOS and PMOS structures in parallel which generates full swing signal at the output with more circuit robustness. As more number of PMOS transistors is utilized, the number of nodes becomes high with increase in area & power and leading in substantial capacitive loads with increase in delay & power. Due to combination, DPL is not considered to be competitive as compared to other pass-transistor logic circuits and complementary CMOS [12].

A DPL is the next version of CPL which alleviates the problems of CPL such as noise margin and speed degradation at reduced supply voltages. Implementation of DPL with high gate capacitance avoids the size issue with full static circuits and n-MOSFET minimal voltage drop issue of the CPL design by utilizing p-MOSFET and n-MOSFET both for pass gates. Similarly a DPL with low-power consumption can be designed by combining the two gates into a single gate excluding the feedback p-MOSFET.

Because CPL uses only NMOS transistors, so it results in low input capacitance with high-speed operation which was caused due to high output signal level and by the NMOS minimal voltage**.** One can use CMOS pass-transistor logic to avoid the problem. Full phase operation is carried out by adding NMOS transistors in parallel to PMOS transistors which results increase in input capacitance.

DPL Full Adder Cell

In this section observation was made on basis of speed of the DPL structure using a full adder. By taking XOR/XNOR gates, a multiplexer and a CMOS output buffer, sum output stage is constructed. Similarly by taking AND/NAND gates, OR/NOR gates, a multiplexer and a CMOS output buffer, carry output stage is constructed. In figure-11, current paths for the outputs when A, B, and *C* are all low are shown by the dark lines. There are two current paths for every output and each path consists of two pass-transistors.

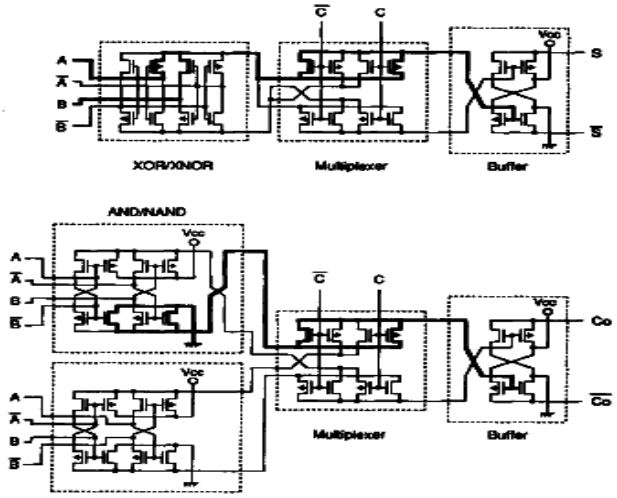

Figure-11: Block diagram of a DPL full Adder cell

It is observed during the comparison that, full adder designed with DPL technique gives same speed as CPL, 38% more quicker than CMOS and 19% more quicker than the conventional pass-transistor logic structure. ALU speed is prove to be the fastest among all and is determined through the carry output delays *(C - CO and A – CO).* But it is found that the pass-transistor architectures gives slightly more power dissipation than CMOS because of the dual rail structure and twice of load capacitance. Here load capacitance is the main component through which it can be determined about the particular architecture which dissipates the smallest amount power. In DPL technique, one type of pass-transistor is controlled by A where it operates in similar fashion like CMOS and CPL. and other is controlled by B. Passing of A is depends on the status of B either low or high. Hence to drive the buffer stage, there are two current paths. Figure-12 shows the schematic and

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figure-13 shows the layout design of the 4-bit DPL full adder cell.

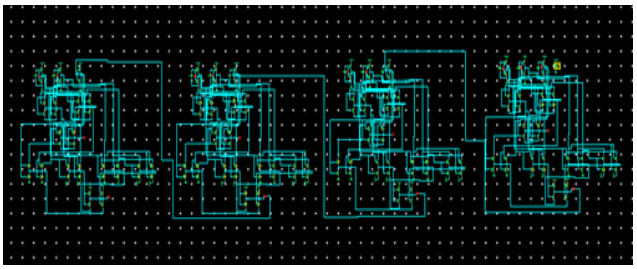

Figure-12: Schematic diagram of a 4-bit DPL Full Adder cell

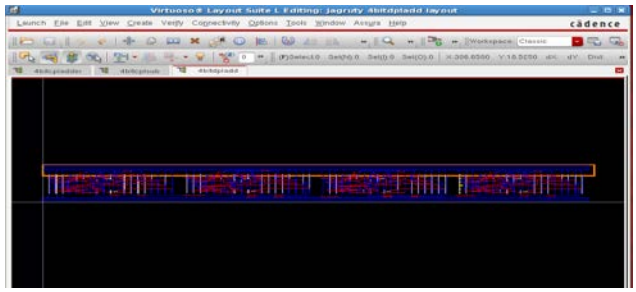

Figure-13: Layout design of a 4-bit DPL Full Adder cell

DPL Full Subtractor Cell

In this part, the design of full subtractor with DPL technique was presented where transistors are independently controlled. Here different conditions like advantages in delay, power consumption, area of fabrication and leakage behavior was considered. Here the count of transistor and area is reduced significantly for logic gates; which tend to increase in logic density per area. For low power consumption, both transistor gates are to be on the same potential even if they are offering less leakage current for getting high performance circuit patterns. But for the lower driving current at the node of operation increases the delay. Figure-14 shows the schematic and figure-15 gives the layout design of a 4-bit DPL full subtractor structure.

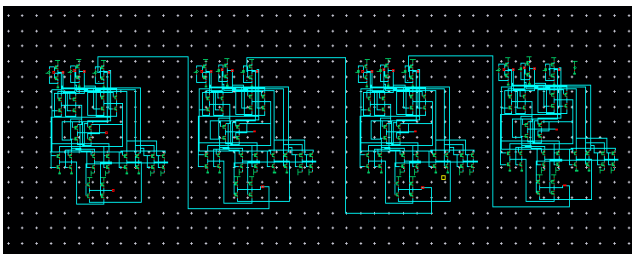

Figure-14: Schematic diagram of a 4-bit DPL Full Subtractor cell

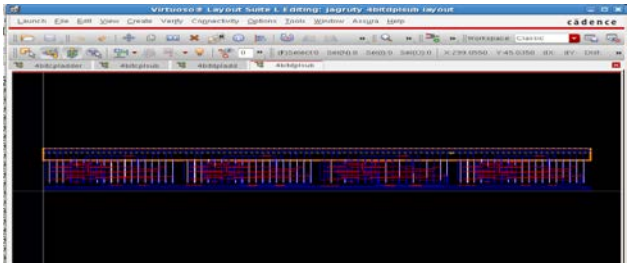

Figure-15: Layout design of a 4-bit DPL Full Subtractor cell

DPL Multiplier Cell

As the binary multiplier circuit is heavily used, the design is made for achieving high performance with better efficiency. Clock frequency plays a vital role to provide maximum delay in any operation. Therefore, the consumption of time in the multiplier circuit plays a massive effect on the speed of the processing element. As observed, the DPL multiplier circuit structure is the fastest known multiplier. Figure-16 gives the schematic of 4X4 DPL multiplier structure.

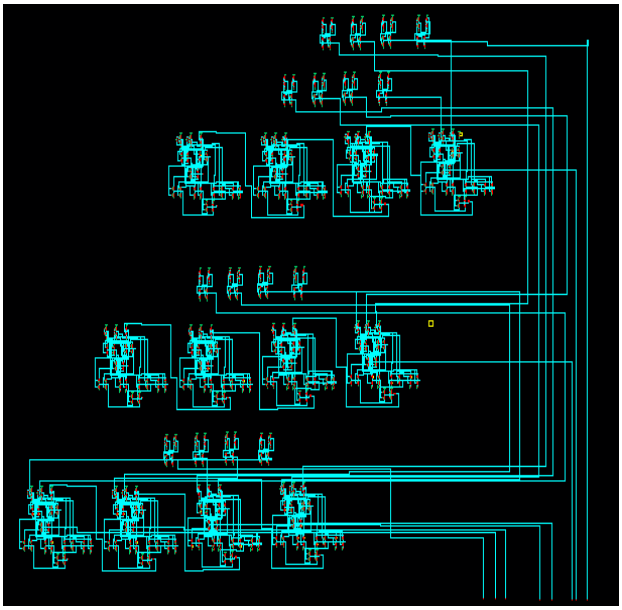

Figure-16: Schematic diagram of a 4X4 DPL Multiplier cell

3.3 Dual Value Logic

To overcome the disadvantages in the DPL gate structure i.e Compensation of speed degradation due to the use of PMOS transistors and the straight forward full swing operation, the new design of logic gate was made which represents an improvement over DPL family and was

achieved by the removal of the redundant branches and reorganization of signals. This is implemented by achieving the following three steps:

Step-1: Removal of the redundant branches

The redesign is carried out by removing the redundant branches from DPL structure. It was carried out mostly by considering the pull up and pull down transition times in the resulting structure by exceed those of the DPL structure gates. The modified gate produces some unwanted input configurations where instead of supplying the current path in two pass-transistors, one transistor is used as DP for making this transition time poorer. Because of one PMOS transistor, degradation of delay takes place and for this width of the same transistor is enlarged. The removal of redundant branches is specified on figure-17. Here the speed of the resulting two halves constituted by the gate is different. The slower half speed is in case of AND gate is 70ps and the faster half speed in case of NAND gate is 60ps and is found to be faster than the DPL case where it is 75ps.

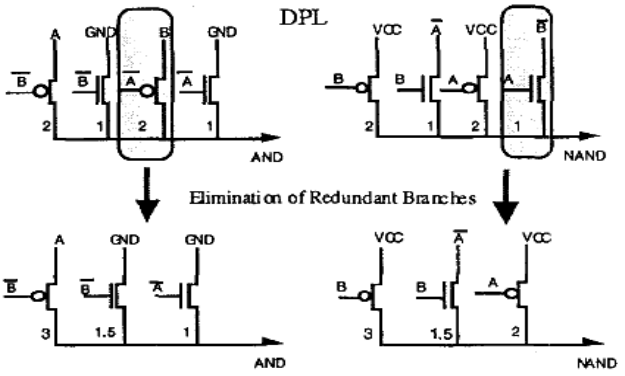

Figure-17: Removal of redundant branches

Step-2: Signal reorganization

Especially in pull up function, the use of dual PMOS transistor provides additional delay compared to parallel use of single NMOS and single PMOS transistor. The current in the structure is the current is always generated either through single NMOS transistor or through parallel configuration of both NMOS and PMOS transistor. Figure-18 shows the DPL gate structure for AND/NOR gates and is formulated from DPL gate structure of NOR/OR with inverted inputs. Here signal reorganization takes place in DPL gate structure of AND/NOR and it is found that the result of AND gate DPL structure is faster. It is obtained 60ps in place of 75ps. So AND is a faster half.

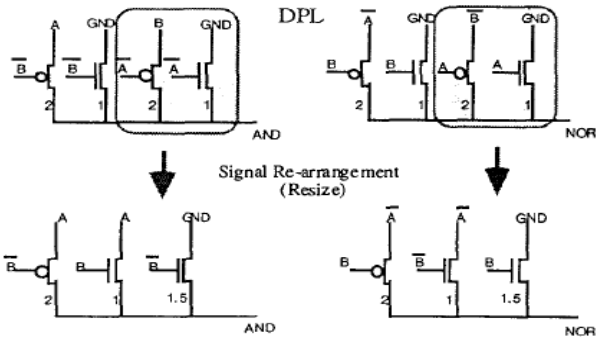

Figure-18: Signal Reorganization

Step-3: Selection of the faster halves

Faster half is now selected as figure-19 where complementary logic gate of the resulting AND/NAND is produced by the removal of redundant branches for the NAND gate and reorganization of signals for AND gates. The new logic is named as Dual Value Logic (DVL). The new DVL gate structure for AND/NAND gate consists of six transistors where it contains four transistors of individual type as compared to DPL gate structure. The DVL gate structure has nine inputs out of which three inputs are for transistor source and other three each inputs are for the p-type and n-type gates respectively where there is twelve inputs in case of DPL gate structure out of which four inputs are for transistor source and for inputs each for p-type and n-type gate of transistors which results small capacitive load at DVL gate structure.

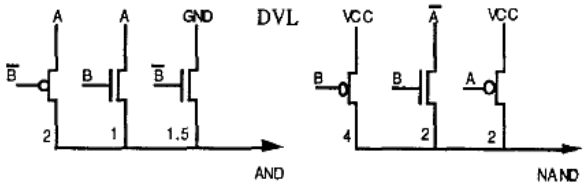

Figure-19: Reorganization of DVL gate structure

The main advantage of DVL structure is employment of Karnaugh-Map at the transistor level. Here functions are formulated directly by utilizing various transistors in series rather than cascading several logic gate like NAND/AND or NOR/OR. For simplification the choice of pseudo Karnaugh-Map in the programming is carried out for less than 8 inputs.

The design of Dual value logic was developed to get advantages over conventional CMOS and new pass-

transistor families like Complementary pass-transistor logic and Double pass-transistor logic. The exact speed enhancement can be determined on each particular type of circuit. It was observed that the consumption of power is reduced to 30% as compared to conventional CMOS where it is 50%. Figures from 20 to 24 shows the schematic and layout design of DVL full adder, DVL full subtractor and DVL multiplier structures respectively.

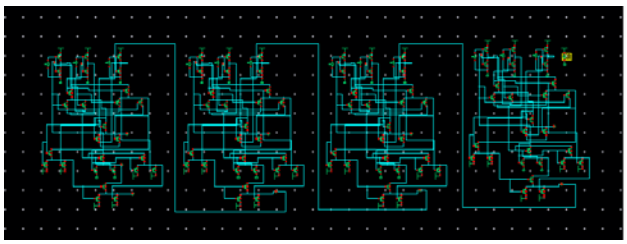

Figure-20: Schematic diagram of a 4-bit DVL Full Adder cell

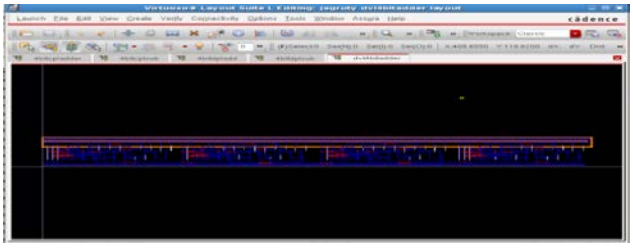

Figure-21: Layout design of a 4-bit DVL Full Adder cell

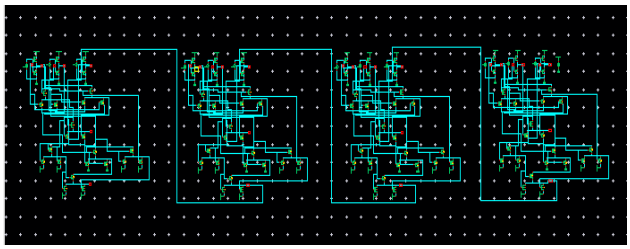

Figure-22: Schematic diagram of a 4-bit DVL Full Subtractor cell

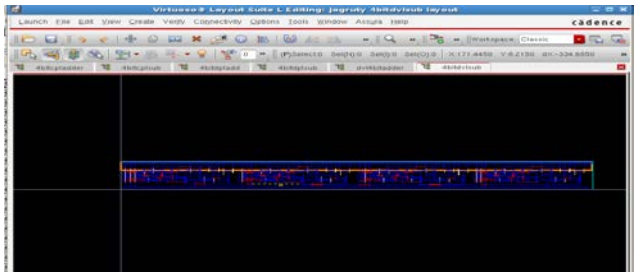

Figure-23: Layout design of a 4-bit DVL Full Subtractor cell

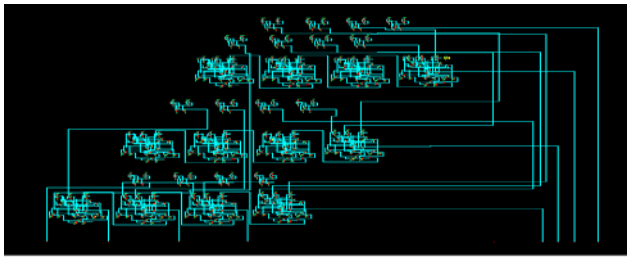

Figure-24: Schematic diagram of a 4X4 DVL Multiplier cell

Result analysis

As CPL utilizes lesser transistors to implement the logic functions, the partial swing at the intermediate nodes wastes more than 50% of power. To avoid this it was proposed to reduce *Vt* of the n-channel MOSFET pass-transistors but it produces reduction in the noise margin to a minimum level which is unacceptable at low supply voltages. Then an extra feedback p-channel MOSFET at the inverter stage is combined and found development by a factor of 2.62 in energy efficiency and a 59% decrease in area as compared to the conventional CPL. As there are both n-MOSFET and p-MOSFET devices are present, so all nodes in DPL structure found to be at full voltage swing and no issue of static short-circuit current. Progress in performance is observed due to two current paths in DPL structure implementation. By applying same technique except feedback p-MOSFET in CPL, it is found that the improvement in DPL's energy efficiency by a factor of 1.55 with a 58% reduction in area as compared to the DPL.

Finally DVL logic structure has been designed to overcome the drawbacks of conventional CMOS and pass-transistor families like CPL & DPL. The exact speed enhancement can be determined on each particular type of circuit. It was observed that the consumption of power is reduced to 30% as compared to conventional CMOS where it is 50%. Obtaining Dual Value Logic structure is formulated by an automated synthesis tool based on the required algorithm.

Conclusion

The importance of combinational circuits for mathematical use is carried out in design of Arithmetic Logic Unit through different logical structures. The design is considered on the low-power implementation techniques. Various methods are presented and examined during the process where it is found that performance of Dual Value Logic is more efficient in energy consumption as compared to Double-pass transistor logic method and

Complementary-pass-transistor logic method. All these three methods using CMOS technology are examined with cadence spectra simulation; it is observed that, the method produced simulation time of 1000ns at a supply voltage of 1.8v.

References

[1] Uming Ko, Balsara, P.T.and Wai Lee, "Low-power design techniques for high-performance CMOS adders", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.3, no.2, pp.327-333, June 1995

[2] Suzuki M., Ohkubo N, Shinbo T, Yamanaka T, Shimizu A, Sasaki K and Nakagome Y, "A 1.5-ns 32-b CMOS ALU in double pass-transistor logic", , *IEEE Journal of Solid-State Circuits*, vol.28, no.11, pp.1145-1151, Nov 1993

[3] Zimmermann Reto and Fichtner Wolfgang, "Low-power logic styles: CMOS versus pass-transistor logic," *IEEE Journal of Solid-State Circuits* , vol.32, no.7, pp.1079, Jul 1997

[4] Oklobdzija V.G and Duchene B, "Pass-transistor dual value logic for low-power CMOS", *Proceedings of Technical Papers. In International Symposium on VLSI Technology, Systems, and Applications*, pp.341-344, 31 May-2 Jun 1995

[5] A. P. Chandrakasan and R. W. Brodersen, "Low Power Digital CMOS Design", *Kluwer, Norwell*, MA, 1995.

[6] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings", *IEEE J. Solid-State Circuits*, vol. 32, pp. 62–69, Jan. 1997

[7] C. Nagendra, R. M. Owens and M. J. Irwin, "Power-delay characteristics of CMOS adders." *IEEE Trans. VU1 System*, vol 1, 1994

[8] Englewood Cliffs and N. Arora, "MOSFET Models for VLSI Circuit Simulation", *Springer-Verlag, Wien, Austria, 1993NJ, 1996J. Solid-State Circuits*, vol. 22, pp. 528–532, Aug. 1987

[9] Santanu Maity, Bishnu Prasad De and Aditya Kr. Singh, "Design and implementation of low power high performance carry skip adder" *International Journal of Engineering and Advanced Technology*, Vol-1, Issue-4, April 2012

[10] Yano K., Yamanaka T, Nishida T, Saito M, Shimohigashi K and Shimizu A,"A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic," *IEEE Journal of Solid state circuits*, vol.25, no.2, pp.388-395, Apr 1990

[11] Abu Khater I.S, Bellaouar A and Elmasry M.I, "Circuit techniques for CMOS low-power high-performance multipliers," *IEEE Journal of Solid state circuits*, vol.31, no.10, pp.1535-1546, Oct 1996

[12] N. Ohkubo *et al.*, "A 4.4 ns CMOS 54 _54-b multiplier using pass transistor multiplexer", *IEEE Journal of Solid state circuits*, vol. 30, pp. 251–257, Mar. 1995

[13] Baker and R. Jacob," CMOS: Circuit Design, Layout, and Simulation", Wiley-IEEE Third Edition.. pp. 1174, 2010

[14] Weste Neil H. E and Harris David M," CMOS VLSI Design: A Circuits and Systems Perspective", Boston: Pearson/Addison-Wesley Fourth Edition, pp. 840, 2010

[15] Veendrick H. J. M," Nanometer CMOS ICs, from Basics to ASICs", *Springer*. pp. 770, 2017

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