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8 Transistor and Modified 8 Transistor Full Adders for Low Power Design

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***Abstract* — The increasing demand for the high fidelity portable devices has laid emphasis on the development of low power and high performance systems. In the next generation processors, the low power design has to be incorporated into fundamental computation units, such as adders and multipliers. The aim of this work is to provide new low power solutions for Very Large Scale Integration design. The Conventional CMOS 28 - Transistor, 8 - Transistor, Modified 8 - Transistor full adders are designed and compared their performance. While comparing adders 8 - Transistor and Modified 8 - Transistor adders consuming less power, delay and Power Delay Product. The simulation has been carried out on TANNER EDA tool using 250nm technology.**

***Index Terms* — Conventional CMOS 28 - Transistor adder, Low power design, Modified 8 - Transistor Adder, and 8 Transistor Adder.**

I. INTRODUCTION

With the rapid development of portable digital applications, the demand for increasing speed, compact implementation, and low power dissipation triggers numerous research efforts. The role of power dissipation in VLSI systems is pervasive. For high performance design, power dissipation can be the limiting factor to clock speed and circuit density because of the inability to get power to circuits or to remove the heat that they generate. For portable information systems, power dissipation has a direct bearing on size, weight, cost, and battery life. Consequently, power dissipation is becoming widely recognized as a top-priority issue for VLSI circuit design.

The challenge facing the VLSI designer is to find and effectively apply circuit techniques that can balance the needs for performance with those of power dissipation. Therefore ultra low power circuits design becomes the major candidates for portable applications.

One common technique for reducing power is power supply scaling. For CMOS circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss somewhat but results in increased leakages. Other techniques used in low power design include clock gating and dynamic voltage / frequency scaling. The rest of the paper is organized as follows: In section II, we briefly describe the previous works on full adders. In section III we describe the modified full adder design. In Section IV and V, the simulation setup and simulation results are presented and discussed. Section VI is the conclusion.

II. ADDER MODULES

Adders are the fundamental building blocks in all the multiplier modules. Hence employing fast and efficient full adders plays a key role in the performance of the entire system. In the following section briefly describe the adder modules used in our design.

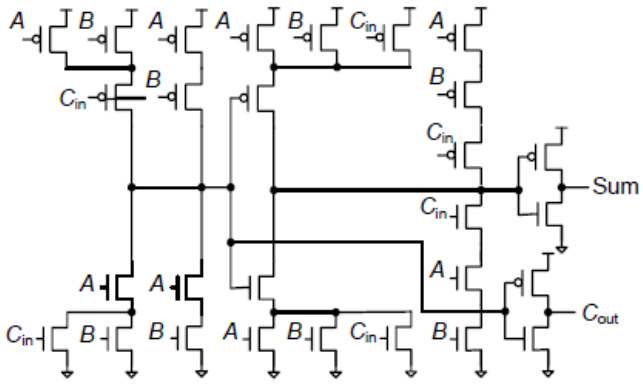

Fig. 1. Conventional CMOS 28-Transistor Adder

A. Conventional CMOS 28-Transistor Full Adder

The 28 - Transistor full adder is the pioneer CMOS traditional adder circuit. The schematic of this

adder is shown in Fig.1. This adder cell is built using equal number of N-FET and P-FET transistors. The logic for the Complimentary MOS logic was realized using the Equation (1) and (2).

$$C_{out} = AB + BC_{in} + AC_{in} \quad (1)$$

$$Sum = ABC_{in} + (A + B + C_{in})\overline{C_{out}} \quad (2)$$

The first 12 transistors of the circuit produce the C_{out} and the remaining transistors produce the Sum outputs. Therefore the delay for computing C_{out} is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area.

B. 8 - Transistor Full Adder

Full adder circuit has been implemented by two XNOR gates and one multiplexer. Sum is generated by two XNOR gates and C_{out} is generated by two transistors multiplexer block. The single bit full adder using proposed XNOR gates with eight transistors has been implemented. Using SPICE simulation the 8 - Transistor has been implemented.

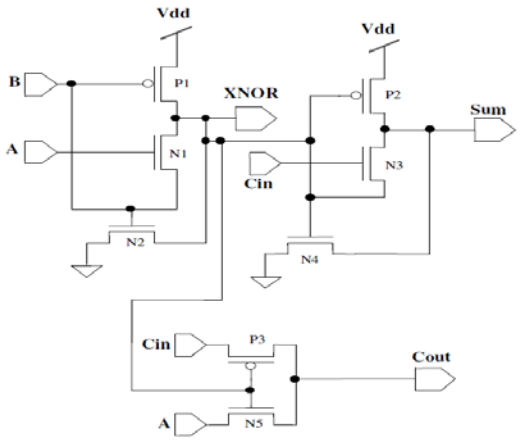

Fig. 2. 8 - Transistor Full Adder

III. PROPOSED METHOD

A. Modified 8-Transistor Full Adder

Full adder circuit can be implemented with different combinations of XOR/XNOR modules and two multiplexer [2, 17] but this approach has not been used in current work as proposed XNOR/XOR cell shows high power consumption than single XNOR gate. Proposed full adder circuit has been implemented by two XNOR gates and one multiplexer block as shown in block diagram of Fig. Sum is generated by two XNOR gates and C_{out} is generated by two transistors multiplexer block.

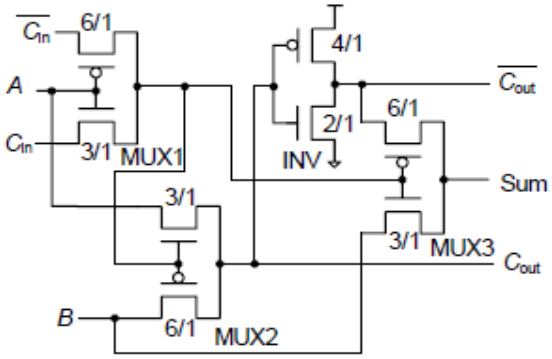

Fig. 3. Modified 8 - Transistor Adder

B. Simulation Setup

The functionality of each of the circuits designed was verified using simulation. The schematics were designed using TANNER EDA tool with 250nm technology. All the adders were analyzed for power consumption, delay and PDP. To yield appropriate results, we have added CMOS inverters at the input and output. While measuring the power and delays, have taken only the input driver into consideration and ignored the output buffer. The power dissipated in CMOS digital circuits is given by Equation (3).

$$P = \alpha C V_{dd}^2 f + I_{sc} * V_{dd} + I_{leak} * V_{dd} \quad (3)$$

Where C is the load capacitance, is the switching activity, f is the clock frequency, *Vdd* is the supply voltage of the system, *I*sc is the short circuit current and *Ileak* is the leakage current of the circuit. The delay measurements for each of the multipliers were averaged for 25 simulation runs and always the worst case delay was taken into consideration. The Effective gate length, Gate oxide thickness, Threshold voltage, Drain Source parasitic resistance are the important parameter in low power design.

C. Simulation Results

In this section, performance measurement of all the three adders has been compared. The design constraints were the same for all the adders. Though low power is the objective of our design, we wanted to measure the delay and power of these circuits, as they are indicators of good performance.

A. Power

The Power consumption for all the adders are investigated and presented in Table I for a 250nm technology size. The Modified 8 - Transistor adder consumed considerably less energy compared to the CMOS adder and 8 - Transistor full adder.

Adder Model	Technology	Power
28-T	250nm	0.0330
8-T		0.00698
Modified 8-T		0.000927

Table 1. Power Comparison (µW)

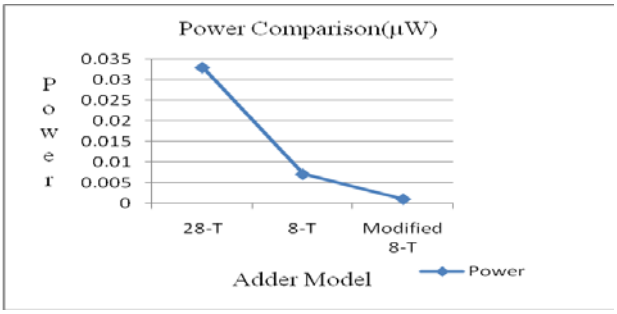

Fig.4. Power Comparison Results

B. *Delay*

Propagation delay is a measure of the speed performance of a circuit, even while consuming low power. In Table II, the delay performance characteristics of various adders used for our study at 250nm technology size are given. For all adders, The Modified 8 - Transistor adder has less delay compared to the CMOS adder and 8 - Transistor full adder.

Adder Model	Technology	Delay
28-T	250nm	2.11
8-T		1.53
Modified 8-T		1.11

Table 2. Delay Comparison (sec)

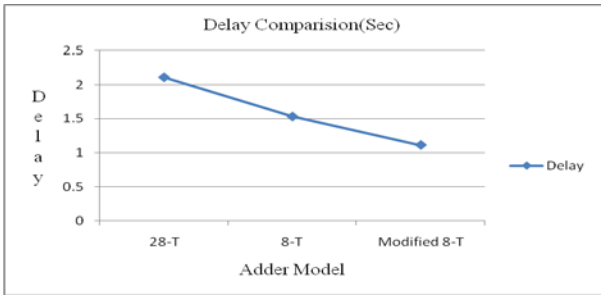

Fig.5. Delay Comparison Results

C. Power Delay Product

The Power-Delay product is the product of Power consumption and the time delay. The smaller value of the Power - Delay product yields the better performance of the design. Since the results shows that the Modified 8 - Transistor adder has less Power Delay Product compared to the CMOS adder and 8 - Transistor full adder.

Adder Model	Technology	PDP
28-T	250nm	69.63
8-T		10.68
Modified 8-T		1.03

Table 3. Power Delay Product

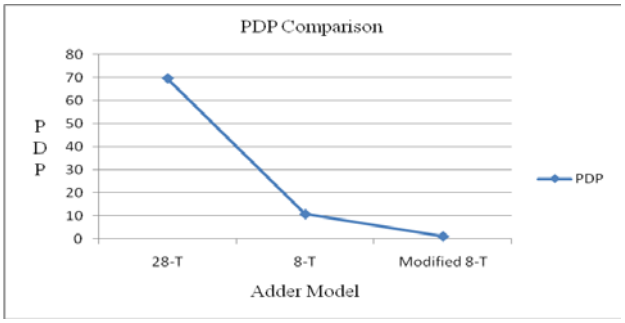

Fig.4. PDP Comparison Results

IV. CONCLUTION

In this paper, the power and delay performance characteristics of three different adders are realized such as 8T, Modified 8 - Transistor and CMOS 28 - Transistor static adders. The result shows that the modified 8Transistor consumed less power compared to 8 - Transistor, Conventional CMOS 28 - Transistor full adder. And also it has less delay and Power Delay Product compare to 8 - Transistor, Conventional CMOS 28 - Transistor full adders. So the Modified 8 - Transistor full adder is well suitable for ultra low power applications at smaller geometry sizes.

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