IJISET - International Journal of Innovative Science, Engineering & Technology, Vol. 8 Issue 8, August 2021
ISSN (Online) 2348 – 7968 | Impact Factor (2020) – 6.72
www.ijiset.com

Evolution of Junctionless Field Effect Transistors in Semiconductor Industry: A Review

[*] Sameeksha Munjal
Department of Electronics and Communication
Punjab Engineering College (Deemed to be university)
sameekshamunjal.phd19ece@pec.edu.in
*Corresponding Author

Dr. Neelam Rup Prakash
Department of Electronics and Communication
Punjab Engineering College (Deemed to be university)
neelamrprakash@pec.edu.in

Dr. Jasbir Kaur
Department of Electronics and Communication
Punjab Engineering College (Deemed to be university)
jasbirkaur@pec.edu.in

Abstract: MOSFET being an integral part of semiconductor industry had played a vital role in its progress. Most important advantage of MOSFET is its device scalability. The scaling of transistor has numerous advantages but when device size reaches submicron regime some undesirable effects come into picture such as lower mobility, short channel effects and gradual change of doping concentration at junctions. The concentration gradient occurring at source/drain junctions increases the complexity of fabricating these devices. To overcome this issue device was introduced called as junctionless FET or gated resistor. The features of junctionless FETs and its characteristics are reviewed in this paper. These devices are uniformly doped nanowires without junctions and has wrap around gate to increase the control over flow of majority carriers in channel thereby increasing the I_{ON} current.

Keywords: Junctionless FETs, MOSFET, operating mode and nanoscale

I. Introduction

Present digital era owes its progress to semiconductor industry. MOSFET being an integral part of the semiconductor industry had played a vital role in its evolution. MOSET has several advantages over its counterpart but one of the important is device scalability. The first MOSFET design in early 1960's had a channel length of 20 µm[1]. Afterwards there is continuous shrinkage in device dimensions in accordance with Moore's Law. Figure 1 demonstrates the exponential increase in number of transistor on chip and decrease in feature size of MOSFET.

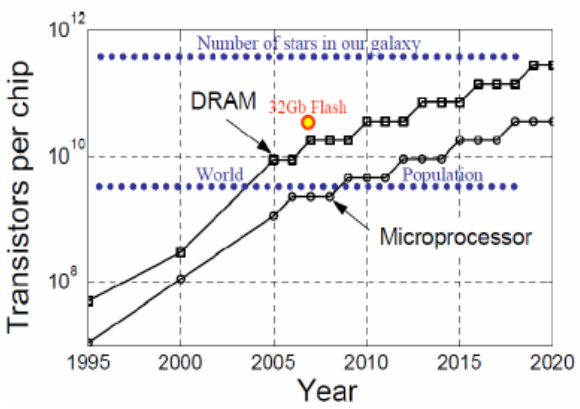


Fig.1 Exponential increase in number of transistor on chip and decrease in feature size of MOSFET[2]

The shrinking of transistors benefitted the semiconductor industry in countless ways by improving the performance of the electronics devices, has higher processing speed and enhanced features while at same time performance cost ratio has been increased. For example, the number of transistors on microprocessor chip

created by Intel has seen variation from 2300 transistor on Intel 4004 to 10^8 transistor on single chip in recent manufactured processors [3].

However as size of transistor is further reduced and dimensions reaches the submicron regime undesirable effects comes into picture such as short channel effects. Short channel effects (SCE) includes threshold voltage roll-off, gate induced barrier limiting (GIDL), drain induced barrier limiting (DIBL), hot electron effect and power dissipation [4]. Performance of devices has been threatened due to the presence of these effects. Also, MOSFET consists of semiconductor junctions' i.e. p-n junction which is formed by a contact between p-type and n-type semiconductor. With downsizing of transistor, size has been reduced to such an extent that it becomes too difficult to construct p-n junction of high quality.

To endure the further advancement in nanoscale semiconductor devices, various researchers have investigated alternative technologies as well as advance device physics. Several new devices emerges that can work at nonoscale dimension that can manage the pace with Moore's Law such as FinFETs, tunnel FETS and negative capacitance devices which allows greater control over the gate at shorter gate length dimensions. Wrapped gate structures gives better high Ion-Ioff ratios but still there exists the problem of lateral diffusion and launching the dopants locally in source and drain regions in these structure [5, 6]. These modified MOSFET structure requires abrupt change in concentration at source/channel and drain channel p-n junctions and achieving such steep change in concentration is extremely difficult at channel length 5-10 nm. Later, the device has been proposed by Prof. J.P Colinge [7] that does not include junction. The proposed device has simpler fabrication process and channel has same concentration as that of source and drain region. The concentration scaling from source to drain region lies in the range of $10^{18}/cm^3$ to $10^{20}/cm^3$ [2, 8]. The features of Junctionless FET and its architecture is reviewed in this paper.

II. Physical Structure and Operating Principles of JLT

Physical Structure of Junctionless FET:

The basic structure of JLT is shown in figure 2.

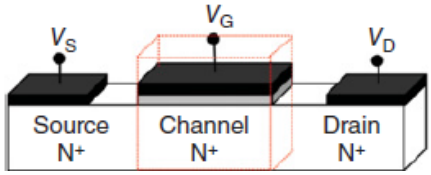


Fig. 2 JLT Structure

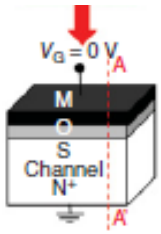


Fig 3 MOS Capacitor of JLT [10]

Unlike MOSFETs, in junctionless transistors p-n junctions are absent and heavily doped thin film is present below the gate region between source and drain region [2, 7]. The semiconductor film has same concentration as that of source drain. The semiconductor film below the gate region modulates the carrier concentration of channel through the applied gate voltage and therefore, modifies the resistivity of channel. As semiconductor film is having same type of concentration as source and drain, therefore no metallurgical pn junction are present

in device unlike other FET devices. Current conduction mechanism of junctionless is different from other device because of the lack of source and drain junctions [8 -9]

Conduction Mechanism:

When electric field is applied to the gate it results in the modulation of carriers from source to drain. Fig 3 demonstrates the MOS capacitor of junctionless transistor. When metal semiconductor work function difference is positive and fermi level of metal is less compared to semiconductor, it results in formation of electric field from semiconductor region to metal region. This field allows the movement of electrons from semiconductor interface to metal, therefore depleting the interface as shown in fig 4.

(a) (b)

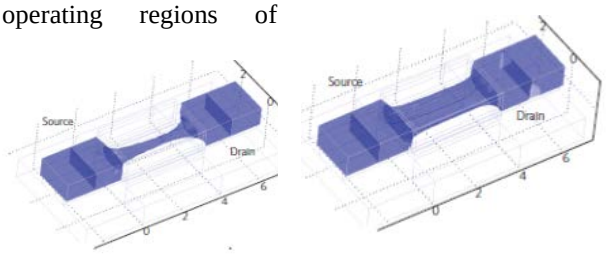
Fig. 4 Energy band (a) before thermal equilibrium and (b) at thermal equilibrium of MOS Capacitor [10]

The complete depletion of semiconductor film is due to the impact of electric field created by gate voltage and it is possible, if film below gate region is thin enough. Entire depletion of semiconductor film is termed as volume depletion or full depletion mode. The gate electrode work function is efficient tool that helps in attaining the volume depletion in junctionless transistor and it operates in off state. When positive gate voltage is applied, it exposes the depleted region and creates the neutral region. This operating region/mode is termed as partially depleted mode where small amount of current flows. The gate voltage below which channel region is completely depleted, this voltage is termed as the threshold voltage for junctionless transistors. The value for threshold voltage for a DGJLFET is given by the equation 1.

$$V_{Th} = V_{FB} - \frac{qN_D t_{Si}^2}{8\varepsilon_{Si}} - \frac{qN_D t_{Si} t_{ox}}{2\varepsilon_{ox}} \quad \text{.....(1)}$$

When gate voltage is further increased, large portion of neutral region will be created and considerable amount of current will flow. This mode of operation of JLT is Flat band mode where majority carriers cause conduction.[7, 9-10].

When applied gate voltage is further increased, then that mode of operation is accumulation mode where there is slight increase in the value of current. JLT are designed to operate in Flat band mode because there are chances of scattering at high value of voltage [9, 11]. Figure 5 illustrates the operating regions of junctionless transistor.



(a) (b)

Fig. 5 Operating modes of JLT (a) Flat band mode and (b) Partial Depltion[11]

III. Historical Background:

Prof. J.P. Colienge [12] in the paper entitled "Junctionless Transistor" communicated about the proposed novel device and all the limitations that are associated with FET structures when they are scaled sown to 10nm. The proposed device named as Junctionless FET or gate resistor, has simpler fabrication and involves fewer steps as compared to that of MOSFET. Thereby, reducing the cost of fabrication of junctionless transistor. In regular MOSFET current flows when channel is inverted and scattering events in inversion mode increase rapidly with increase in applied gate voltage, resulting in decrease in transconductance and current carrying capacity. Figure 6 illustrates the schematic view of multigate JunctionlessFET.

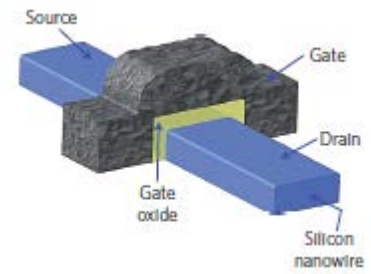


Fig. 6 Schematic view of MuG Junctionless FET [12]

Lee et. al. [13] studied the junctionless transistor for deep submicron technology node. They have simulated both inversion mode (N^+-P-N^+) and accumulated mode junctionless (N^+-N^+-N^+) transistor and concluded that junctionless FET have improved short channel characteristics. Figure 7 shows the subthreshold characteristics at different values of gate length. This shows that JLT has subthreshold slope below 80mV/dec and could be used for submicron applications.

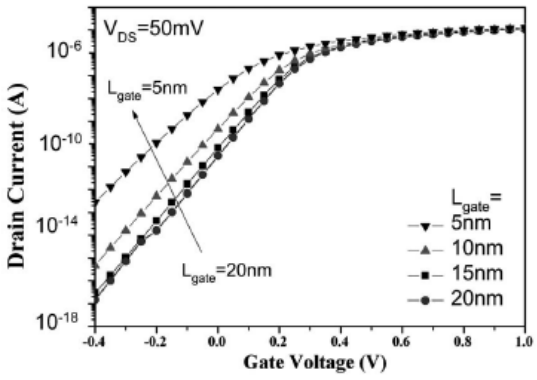


Fig. 7 Subthreshold characteristics of JLT at different gate length [13]

J.P. Colienge [14] compared different types of FET structures and concluded that JLT has similar characteristics of accumulation mode FET. Figure 8 shows the different types of conduction mechanisms in different FET devices. This shows that JLT has been capable of providing large amount of drain current. The value for drain current in Flat band mode for JLT is given by equation 2.

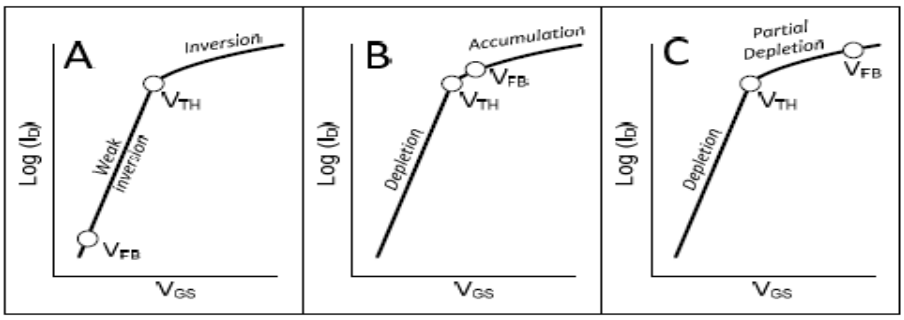


Fig. 8 Conduction Mechanism (A: Inversion Mode FET, B: Accumulated Mode FET and C: Junctionless Transistor) [14]

$$I_D = \frac{q\mu_b N_D}{L_{effb}} S_{max} C_{ox} + \frac{\mu_{acc} C_{ox} W_{eff}}{L_{effacc}} \left(V_{DS}(V_{GS} - V_{FB}) - \frac{1}{2} V_{DS}^2 \right) \quad (2)$$

He also explained that by replacing the channel with heavily doped material same as that of source/drain decreases the boundary potential and results in increase current drive.

Gundapaneni et. al. [15] proposed the use of high-k dielectric for JL device to improve the scalability and electrostatic integrity. JL device was simulated by using spacers of different materials having different values of dielectric constant. Figure 9 demonstrates the I_d-V_{gs} characteristics at different values of dielectric constant.

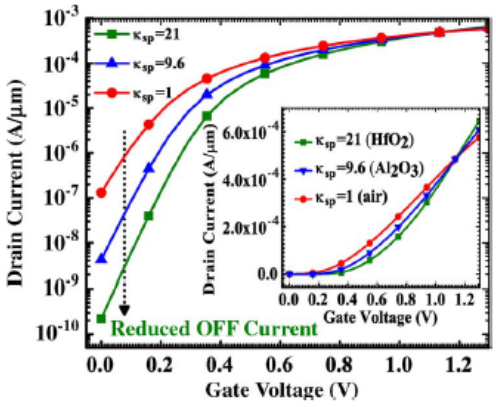


Fig. 9 I_d-V_{gs} characteristics of JL at 20 nm gate length varying dielectric constant from 1 to 21 [15]

They have concluded that use of spacers resulted in enhanced depletion due to the effect of fringing field caused by the spacers used. The enhanced depletion caused the larger barrier at source-channel interface and has higher effective gate length. JL device when integrated with high-k spacers results in reduced leakage current.

Han et. al. [16] explained the temperature dependent characteristics of junctionless FET. They explained the effect the of temperature on drain current (I_d) and gate capacitance (C_{gg}) and varied the temperature from 150K to 500K. Figure 10 demonstrates drain current values at different gate voltages.

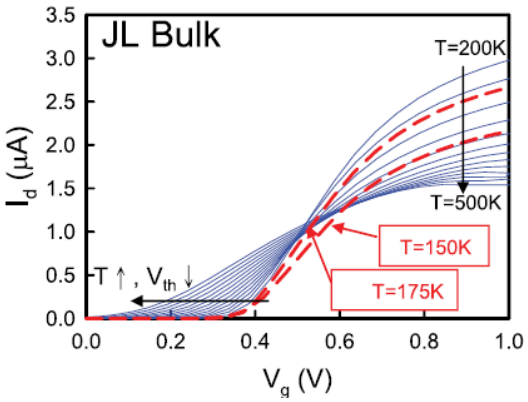


Fig 10. Drain current as a function of gate voltage for JLT [16]

They also concluded that for JL devices impurity scattering dominates, therefore no ZTC had been observed. Gate capacitance is combination of oxide capacitance and semiconductor capacitance in JL device which shows more sensitivity to the temperature as compare to the IM device because semiconductor capacitance is the function of temperature in float band condition and is given by equation 3.

$$C_S = \sqrt{qN_{ch}\frac{q}{kT}\varepsilon_S}, \quad \text{....(3)}$$

Kim et al.[17] implemented junctionless accumulated mode (JAM) MOSFET based on junctioned isolated FIinFET. Figure 11 represents the cross sectional view of JAM FET.

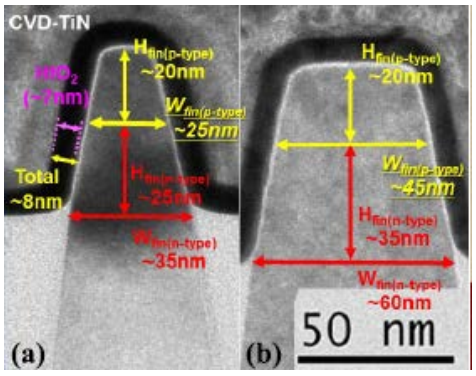


Fig. 11 Cross sectional view of JAM at different fin width (a) W= 25nm (b) W= 50 nm [17]

It has been observed that when channel length or width of fin is increased it resulted in decreased Ion/Ioff ratio. Increased Ion/Ioff ratio is either due to higher value of subthreshold slope or increased channel resistance. This could be depicted from figure 12. Therefore, to obtain the desired characteristics JAM devices either have minimum fin width or maximum value of channel length.

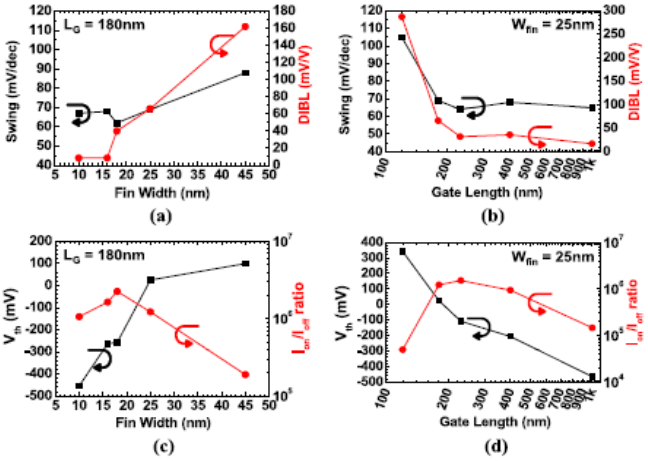


Fig 12 Dependency of parameters on Channel length and fin width.(a) and (c) Simulated at channel length 180 nm (b) and (d) Simulated at fin width 25 nm. [17]

IV. Leakage Current

Leakage current is measured by without applying gate voltage but at the same time drain voltage is applied. Absence of gate voltage is required to decrease the barrier that has been originated due to work function difference between metal and semiconductor. Figure 13 demonstrates the leakage current for junctionless FET at gate length of 20 nm and applied drain voltage was 1.2 V.

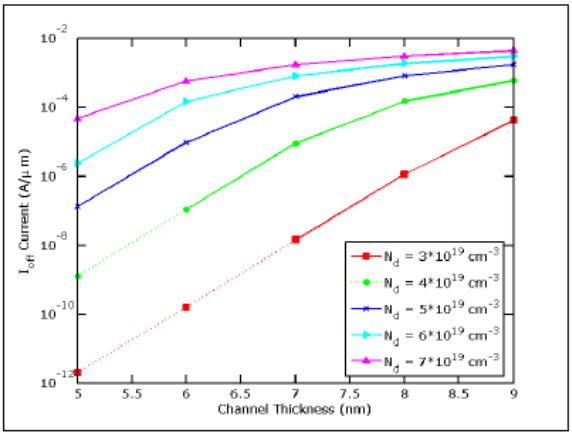


Fig. 13 Ioff current as the function of channel doping concentration and thickness [18]

The results were obtained by Dr. Vitale et. al [18] by performing Monte Carlo simulation. In JLT, the semiconductor film should thin enough to provide high energy barrier for whole source to drain region. The energy barrier attains its maximum value nearer to gate and minimum value when it is far away i.e. at the centre of the channel. It had been observed that when doping concentration of semiconductor film increases, leakage current also increases. Therefore, to obtain the minimum value of leakage current doping concentration should be lower than $4*10^{-19}$ /cm^3.

V. Comparison with Junctioned FETs

DIBL i.e drain induced barrier lowering which measures the amount of drop in energy barrier when drain voltage is applied equal to value which is applied while calculating the Ion current [19]. The relation between the threshold voltage and short channel effects could be understood using the equation 4:

$$V_{th} = V_{tho} - SCE - DIBL \ldots\ldots (4)$$

This equation shows that decrease in the value of threshold voltage in MOSEFET is due to short channel effect and DIBL which is due to space charge region that grows by applying drain voltage. Consider L_{eff} be the effective channel length of MOSFET when it is in on condition and L_{sce} when it is in off state. $L_{eff}>L_{sce}$, therefore, effective gate length is greater when it is in on state. In JLT, doping concentration is same throughout from source to drain. The electrostatic squeezing of the channel transmits into source and drain region in off state, leads to increased effective gate length. When it is operating in off state electrostatic squeezing is absent i.e. L_{eff} is equal to physical gate length. Therefore, JLT has increased effective channel length in off state thereby resulting better short channel effects [20-22]. Figure 14 demonstrates the gate length of JLT in on and aff state.

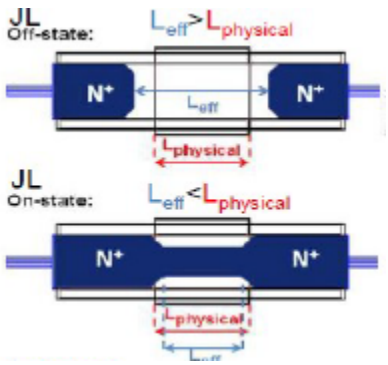


Fig. 14 Gate length of JLT in off state and On –state [2]

In JLT, the electric field produced due to gate voltage which is perpendicular to current flow is lessen as compare to that of inversion mode MOSFETs. This electric field reduces the mobilty of carrier in the channel due to scattering effect. Therefore, JLT has advantage over MOSFETs in terms of current device. At the same time , JLT has simpler fabrication due to eradication of junction implantation and annealing, leading to reduced cost of fabrication [2, 23-25]. Figure 15 illudtrates the simulation of elrctric field for inversion mode and junctionless device Both were simulated in sub threshold region (Vds=1V and gate voltage , Vgs= Vth-200mV). It had been observed that at darin junction electric field has high value which extends to the channel region, causing DIBL to increase and reducing the output impedance [23]. In JLT devices, high electric field is limited to drain region and outside region is covered by gate and peak value of electric filed is lower in junctionless devices. So, it has been concluded that drain electric field has less impact on on the channel region JLT device as compare to junctioned devices, ensuring insignificant DIBL for JLT [25].

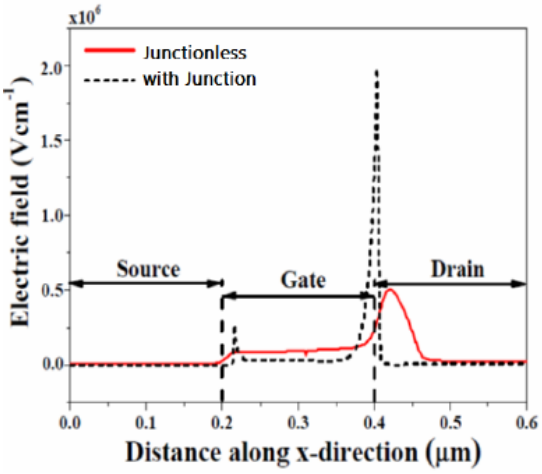


Fig. 15 Drain electric field for JL and Junctioned device [2]

V. Conclusions

This paper reviewed the device named as Junctionless nanowire transistor. The device is either n^+ or p^+ nanowire FET and does not include junctions at source/drain. This eliminates ultrasteep change in concentration at source/channel or drain/channel junction. Therefore, they are less sensitive to short channel effects and have subthreshold slope near to the ideal value. Mobility degradation is less in gated resistor or junctionless transistor as compared to that of regular MOSFET as current flow in the bulk region.

References

[1]. "2015 International Technology Roadmap for Semiconductors (ITRS) - Semiconductor Industry Association." [Online]. Available: https://www.semiconductors.org/resources/2015-international-technology-roadmap-for-semiconductors-itrs/

[2]. R. Singh and S.K. Yadav, "Analysis and Comprehensive study of Junction-less transistor," *Int. J. Eng. Sci Adv Research*, vol. 4, no. 2, pp. 1–8, 2018.

[3]. M. H. Bhuyan, "History and Evolution of CMOS Technology and its Application in Semiconductor Industry," *SEU J. Sci. Eng.*, vol. 11, no. 1, pp. 30–42, 2017.

[4]. J. Rabaey, Low Power Design Essentials. Boston, MA: Springer US, 2009.

[5]. M. Riyadi, J. Suseno, and R. Ismail, "The future of Non-planar Nanoelectrponics MOSFET Devices: A Review," *J. Appl. Sci.*, vol. 10, no. 18, pp. 2136–2146, 2010.

[6]. P. Agnihotri and N. Tripathi, "Junctionless Transistors for Future Applications," *Int. J. of Information Technol. and Electrical Eng.*, vol. 8, no. 4,2020.

[7]. J. P. Colinge et al., "Nanowire transistors without junctions," Nat. Nanotechnol., vol. 5, no. 3, pp. 225–229, 2010.

[8]. S. Sahay; M. Jagadesh Kumar, "Introduction to Field Effect Transistors," in Junctionless Field-Effect Transistors: Design, Modeling, and Simulation , IEEE, 2019, pp.1-26, doi: 10.1002/9781119523543.ch1.

[9]. S. Sahay; M. Jagadesh Kumar, "Fundamentals of Junctionless Field Effect Transistors," in Junctionless Field-Effect Transistors: Design, Modeling, and Simulation , IEEE, 2019, pp.67-123, doi: 10.1002/9781119523543.ch3.

[10]. C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 13–15, 2009.

[11]. J. P. Colinge *et al.*, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid. State. Electron.*, vol. 65–66, no. 1, pp. 33–37, 2011.

[12]. J. P. Colinge *et al.*, "Junctionless Transistors: Physics and Properties," Semiconductor-On-Insulator Materials for Nanoelectronics Applications, 2011, pp. 187–200.

[13]. C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J. P. Colinge, "Junctionless multigate field-effect transistor," *Appl. Phys. Lett.*, vol. 94, no. 5, pp. 13–15, 2009.

[14]. J. P. Colinge, "Junctionless transistors," IMFEDK 2012 - 2012 *Int. Meet. Futur. Electron Devices, Kansai*, pp. 20–21, 2012

[15]. S. Gundapaneni, S. Ganguly, and A. Kottantharayil, "Enhanced electrostatic integrity of short-channel junctionless transistor with high-κ spacers," *IEEE Electron Device Lett.*, vol. 32, no. 10, pp. 1325–1327, 2011.

[16]. M. H. Han, H. Bin Chen, S. S. Yen, C. S. Shao, and C. Y. Chang, "Temperature-dependent characteristics of junctionless bulk transistor," *Appl. Phys. Lett.*, vol. 103, no. 13, pp. 101–104, 2013.

[17]. T. K. Kim, et al., "First Demonstration of Junctionless Accumulation-Mode Bulk FinFETs With Robust Junction Isolation," *IEEE Electron Device Lett.*, pp. 1-3, 2013.

[18]. W. Vitale, M. Mohamed, and U. Ravaioli, "Monte Carlo study of transport properties in junctionless transistors," *2010 14th Int. Work. Comput. Electron. IWCE 2010*, pp. 243–245, 2010.

[19]. J.H. Choi, *et al.*, "Origin of Device Performance Enhancement of Junctionless Accumulation-Mode (JAM) Bulk FinFETs With High-*κ* Gate Spacers," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 1182–1184, Dec. 2014.

[20]. S. Lee, J. Lee, and S. Cho, "Design and characterization of electrically self-isolated GaN-on-Si junctionless fin-shaped channel field-effect transistor with higher cost-effectiveness for low-power applications," *Jpn. J. Appl. Phys.*, vol. 54, no. 8, pp. 0–6, 2015.

[21]. T. Solankia and N. Parmar, "A Review paper : A Comprehensive study of Junctionless transistor," *Natl. Conf. Recent Trends Eng. Technol.*, no. May, pp. 1–5, 2011.

[22]. C. H. Park *et al.*, "Comparative study of fabricated junctionless and inversion-mode nanowire FETs," *Device Res. Conf. - Conf. Dig. DRC*, vol. 41, no. 4, pp. 179–180, 2011.

[23]. C. H. Tai, J. T. Lin, Y. C. Eng, and P. H. Lin, "A novel high-performance junctionless vertical MOSFET produced on bulk-si wafer," *ICSICT-2010 - 2010 10th IEEE Int. Conf. Solid-State Integr. Circuit Technol. Proc.*, vol. 3, pp. 108–110, 2010.

[24]. R. Duffy, "The (R)Evolution of the Junctionless Transistor," *ECS Trans.*, vol. 72, no. 4, pp. 115–126, 2016.

[25]. J. Alamo, et al., " Nanometer-Scale III-V MOSFETs," *IEEE J.Electron Devices Society*, vol.4 pp.205-214, Sep. 2016.